40MX and 42MX FPGA Families

Actel now offers a '–3' speed grade option for the A42MX09, A42MX16, A42MX24, and A42MX36 devices.

This addendum contains only the '–3' speed grade numbers. For '–2', '–1', 'Std', and '–F' numbers, please refer to the Timing Characteristics Tables on pages 47 through 72 in the standalone *40MX and 42MX FPGA Families* data sheet and on pages 145 through 170 of the *1999 Actel FPGA Data Book*.

A42MX09 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.20	ns
t_{CO}	Sequential Clock-to-Q		1.29	ns
t_{GO}	Latch G-to-Q		1.23	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.24	ns
Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		0.69	ns
t_{RD2}	FO=2 Routing Delay		0.92	ns
t_{RD3}	FO=3 Routing Delay		1.15	ns
t_{RD4}	FO=4 Routing Delay		1.38	ns
t_{RD8}	FO=8 Routing Delay		2.34	ns
Sequential Timing Characteristics[3, 4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.32		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.41		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.39		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.45		ns
t_A	Flip-Flop Clock Input Period	3.45		ns
t_{INH}	Input Buffer Latch Hold	0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.27		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.27		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		268.13	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.04	ns
t_{INYL}	Pad-to-Y LOW			0.82	ns
t_{INGH}	G to Y HIGH			1.29	ns
t_{INGL}	G to Y LOW			1.29	ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			2.02	ns
t_{IRD2}	FO=2 Routing Delay			2.26	ns
t_{IRD3}	FO=3 Routing Delay			2.50	ns
t_{IRD4}	FO=4 Routing Delay			2.75	ns
t_{IRD8}	FO=8 Routing Delay			3.72	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 256		2.43 2.70	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 256		3.53 3.87	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 256	1.22 1.31		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 256	1.22 1.31		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.31 0.31	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 256	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	2.34 2.19		ns ns
t_P	Minimum Period	FO = 32 FO = 256	3.35 3.69		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		295.63 268.13	MHz MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance*

A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		2.44	ns
t_{DHL}	Data-to-Pad LOW		2.87	ns
t_{ENZH}	Enable Pad Z to HIGH		2.64	ns
t_{ENZL}	Enable Pad Z to LOW		2.92	ns
t_{ENHZ}	Enable Pad HIGH to Z		4.90	ns
t_{ENLZ}	Enable Pad LOW to Z		5.34	ns
t_{GLH}	G-to-Pad HIGH		2.61	ns
t_{GHL}	G-to-Pad LOW		2.61	ns
t_{LSU}	I/O Latch Set-Up	0.49		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.20	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.36	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		2.44	ns
t_{DHL}	Data-to-Pad LOW		2.87	ns
t_{ENZH}	Enable Pad Z to HIGH		2.64	ns
t_{ENZL}	Enable Pad Z to LOW		2.92	ns
t_{ENHZ}	Enable Pad HIGH to Z		4.90	ns
t_{ENLZ}	Enable Pad LOW to Z		5.34	ns
t_{GLH}	G-to-Pad HIGH		4.15	ns
t_{GHL}	G-to-Pad LOW		4.15	ns
t_{LSU}	I/O Latch Set-Up	0.49		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.20	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.36	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.04	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX09 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.62	ns
t_{CO}	Sequential Clock-to-Q		1.80	ns
t_{GO}	Latch G-to-Q		1.69	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.96	ns
Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		0.99	ns
t_{RD2}	FO=2 Routing Delay		1.26	ns
t_{RD3}	FO=3 Routing Delay		1.62	ns
t_{RD4}	FO=4 Routing Delay		1.89	ns
t_{RD8}	FO=8 Routing Delay		3.24	ns
Sequential Timing Characteristics[3, 4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.45		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.57		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.74		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.22		ns
t_A	Flip-Flop Clock Input Period	5.04		ns
t_{INH}	Input Buffer Latch Hold	0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.27		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.27		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		160.93	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.47	ns
t_{INYL}	Pad-to-Y LOW			1.17	ns
t_{INGH}	G to Y HIGH			1.80	ns
t_{INGL}	G to Y LOW			1.80	ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			2.84	ns
t_{IRD2}	FO=2 Routing Delay			3.15	ns
t_{IRD3}	FO=3 Routing Delay			3.51	ns
t_{IRD4}	FO=4 Routing Delay			3.87	ns
t_{IRD8}	FO=8 Routing Delay			5.22	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 256		4.05 4.50	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 256		4.95 5.40	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 256	1.70 1.85		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 256	1.70 1.85		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.42 0.42	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 256	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	3.33 3.69		ns ns
t_P	Minimum Period	FO = 32 FO = 256	5.58 6.12		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		177.43 160.93	MHz MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance*

A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.41	ns
t_{DHL}	Data-to-Pad LOW		4.01	ns
t_{ENZH}	Enable Pad Z to HIGH		3.69	ns
t_{ENZL}	Enable Pad Z to LOW		4.09	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.85	ns
t_{ENLZ}	Enable Pad LOW to Z		7.47	ns
t_{GLH}	G-to-Pad HIGH		5.81	ns
t_{GHL}	G-to-Pad LOW		5.81	ns
t_{LSU}	I/O Latch Set-Up	0.68		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.73	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.15	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.00	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.09	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.42	ns
t_{DHL}	Data-to-Pad LOW		4.05	ns
t_{ENZH}	Enable Pad Z to HIGH		3.69	ns
t_{ENZL}	Enable Pad Z to LOW		4.09	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.85	ns
t_{ENLZ}	Enable Pad LOW to Z		7.47	ns
t_{GLH}	G-to-Pad HIGH		5.81	ns
t_{GHL}	G-to-Pad LOW		5.81	ns
t_{LSU}	I/O Latch Set-Up	0.68		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.73	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.15	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.04	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.05	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX16 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.37	ns
t_{CO}	Sequential Clock-to-Q		1.44	ns
t_{GO}	Latch G-to-Q		1.37	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.57	ns
Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		0.77	ns
t_{RD2}	FO=2 Routing Delay		1.04	ns
t_{RD3}	FO=3 Routing Delay		1.29	ns
t_{RD4}	FO=4 Routing Delay		1.55	ns
t_{RD8}	FO=8 Routing Delay		2.57	ns
Sequential Timing Characteristics[3,4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.32		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.68		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.40		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.46		ns
t_A	Flip-Flop Clock Input Period	6.80		ns
t_{INH}	Input Buffer Latch Hold	0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.49		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.49		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		214.50	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.05	ns
t_{INYL}	Pad-to-Y LOW			0.81	ns
t_{INGH}	G to Y HIGH			1.40	ns
t_{INGL}	G to Y LOW			1.40	ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			1.83	ns
t_{IRD2}	FO=2 Routing Delay			2.09	ns
t_{IRD3}	FO=3 Routing Delay			2.34	ns
t_{IRD4}	FO=4 Routing Delay			2.60	ns
t_{IRD8}	FO=8 Routing Delay			3.63	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 384		2.61 2.88	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 384		3.78 4.46	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 384	3.18 3.65		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 384	3.18 3.65		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.34 0.34	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	2.77 3.18		ns ns
t_P	Minimum Period	FO = 32 FO = 384	4.19 4.61		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		236.50 214.50	MHz MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		2.51	ns
t_{DHL}	Data-to-Pad LOW		2.94	ns
t_{ENZH}	Enable Pad Z to HIGH		2.70	ns
t_{ENZL}	Enable Pad Z to LOW		2.99	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.42	ns
t_{ENLZ}	Enable Pad LOW to Z		5.01	ns
t_{GLH}	G-to-Pad HIGH		2.88	ns
t_{GHL}	G-to-Pad LOW		2.88	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.65	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.03	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.20	ns
t_{DHL}	Data-to-Pad LOW		2.46	ns
t_{ENZH}	Enable Pad Z to HIGH		2.70	ns
t_{ENZL}	Enable Pad Z to LOW		2.99	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.42	ns
t_{ENLZ}	Enable Pad LOW to Z		5.01	ns
t_{GLH}	G-to-Pad HIGH		5.07	ns
t_{GHL}	G-to-Pad LOW		5.07	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.65	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.03	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX16 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

Logic Module Propagation Delays[1]		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		1.92	ns
t_{CO}	Sequential Clock-to-Q		2.02	ns
t_{GO}	Latch G-to-Q		1.92	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.20	ns
Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		1.09	ns
t_{RD2}	FO=2 Routing Delay		1.45	ns
t_{RD3}	FO=3 Routing Delay		1.81	ns
t_{RD4}	FO=4 Routing Delay		2.16	ns
t_{RD8}	FO=8 Routing Delay		3.60	ns
Sequential Timing Characteristics[3, 4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.45		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.00		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.95		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.76		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.24		ns
t_A	Flip-Flop Clock Input Period	9.52		ns
t_{INH}	Input Buffer Latch Hold	0.00		ns
t_{INSU}	Input Buffer Latch Set-Up	0.68		ns
t_{OUTH}	Output Buffer Latch Hold	0.00		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.68		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		128.70	MHz

Notes:

1. *For dual-module macros use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			1.48	ns
t_{INYL}	Pad-to-Y LOW			1.13	ns
t_{INGH}	G to Y HIGH			1.96	ns
t_{INGL}	G to Y LOW			1.96	ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			2.57	ns
t_{IRD2}	FO=2 Routing Delay			2.92	ns
t_{IRD3}	FO=3 Routing Delay			3.28	ns
t_{IRD4}	FO=4 Routing Delay			3.64	ns
t_{IRD8}	FO=8 Routing Delay			5.08	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 384		4.35 4.80	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 384		5.29 6.24	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 384	5.67 6.62		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 384	5.29 6.24		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.48 2.18	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	3.88 4.45		ns ns
t_P	Minimum Period	FO = 32 FO = 384	6.98 7.70		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		141.90 128.70	MHz MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–3' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.52	ns
t_{DHL}	Data-to-Pad LOW		4.12	ns
t_{ENZH}	Enable Pad Z to HIGH		3.78	ns
t_{ENZL}	Enable Pad Z to LOW		4.18	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.58	ns
t_{ENLZ}	Enable Pad LOW to Z		7.01	ns
t_{GLH}	G-to-Pad HIGH		4.77	ns
t_{GHL}	G-to-Pad LOW		4.77	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.25	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		4.48	ns
t_{DHL}	Data-to-Pad LOW		3.44	ns
t_{ENZH}	Enable Pad Z to HIGH		3.78	ns
t_{ENZL}	Enable Pad Z to LOW		4.18	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.58	ns
t_{ENLZ}	Enable Pad LOW to Z		7.01	ns
t_{GLH}	G-to-Pad HIGH		7.10	ns
t_{GHL}	G-to-Pad LOW		7.10	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.25	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX24 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

		Preliminary Information		
Logic Module Propagation Delays[1]		**'–3 Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Combinatorial Functions				
t_{PD}	Internal Array Module Delay		1.18	ns
t_{PDD}	Internal Decode Module Delay		1.43	ns
Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		0.80	ns
t_{RD2}	FO=2 Routing Delay		1.04	ns
t_{RD3}	FO=3 Routing Delay		1.26	ns
t_{RD4}	FO=4 Routing Delay		1.49	ns
t_{RD5}	FO=8 Routing Delay		2.40	ns
Sequential Timing Characteristics[3, 4]				
t_{CO}	Flip-Flop Clock-to-Output		1.29	ns
t_{GO}	Latch Gate-to-Output		1.18	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.32		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.40	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.41		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.31		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.35		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information		
Input Module Propagation Delays			**'–3' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.03	ns
t_{INGO}	Input Latch Gate-to-Output			1.25	ns
t_{INH}	Input Latch Hold		0.00		ns
t_{INSU}	Input Latch Set-Up		0.48		ns
t_{ILA}	Latch Active Pulse Width		4.66		ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			1.83	ns
t_{IRD2}	FO=2 Routing Delay			2.06	ns
t_{IRD3}	FO=3 Routing Delay			2.29	ns
t_{IRD4}	FO=4 Routing Delay			2.52	ns
t_{IRD8}	FO=8 Routing Delay			3.43	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO=32 FO=486		2.61 2.88	ns ns
t_{CKL}	Input HIGH to LOW	FO=32 FO=486		3.65 4.26	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32 FO=486	2.16 2.37		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO=32 FO=486	2.16 2.37		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=486		0.54 0.54	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=486	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=486	2.77 3.31		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32 FO=486	4.71 5.14		ns ns
f_{MAX}	Maximum Datapath Frequency	FO=32 FO=486		210.38 192.50	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Output Module Timing		**'–3 Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		2.43	ns
t_{DHL}	Data-to-Pad LOW		2.84	ns
t_{ENZH}	Enable Pad Z to HIGH		2.54	ns
t_{ENZL}	Enable Pad Z to LOW		2.82	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.15	ns
t_{ENLZ}	Enable Pad LOW to Z		4.80	ns
t_{GLH}	G-to-Pad HIGH		2.88	ns
t_{GHL}	G-to-Pad LOW		2.88	ns
t_{LSU}	I/O Latch Output Set-Up	0.48		ns
t_{LH}	I/O Latch Output Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.47	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.60	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.11	ns
t_{DHL}	Data-to-Pad LOW		2.35	ns
t_{ENZH}	Enable Pad Z to HIGH		2.54	ns
t_{ENZL}	Enable Pad Z to LOW		2.82	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.15	ns
t_{ENLZ}	Enable Pad LOW to Z		4.80	ns
t_{GLH}	G-to-Pad HIGH		4.88	ns
t_{GHL}	G-to-Pad LOW		4.88	ns
t_{LSU}	I/O Latch Set-Up	0.48		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.47	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.60	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.03	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX24 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

		Preliminary Information		
Logic Module Propagation Delays[1]		**'–3 Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Combinatorial Functions				
t_{PD}	Internal Array Module Delay		2.01	ns
t_{PDD}	Internal Decode Module Delay		1.13	ns
Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		1.66	ns
t_{RD2}	FO=2 Routing Delay		2.01	ns
t_{RD3}	FO=3 Routing Delay		1.13	ns
t_{RD4}	FO=4 Routing Delay		1.45	ns
t_{RD5}	FO=8 Routing Delay		1.76	ns
Sequential Timing Characteristics[3, 4]				
t_{CO}	Flip-Flop Clock-to-Output		2.09	ns
t_{GO}	Latch Gate-to-Output		3.37	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.44		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.95	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.57		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.64		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.08		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information		
Input Module Propagation Delays			**'–3' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.44	ns
t_{INGO}	Input Latch Gate-to-Output			1.75	ns
t_{INH}	Input Latch Hold		0.00		ns
t_{INSU}	Input Latch Set-Up		0.67		ns
t_{ILA}	Latch Active Pulse Width		6.53		ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			2.57	ns
t_{IRD2}	FO=2 Routing Delay			2.88	ns
t_{IRD3}	FO=3 Routing Delay			3.20	ns
t_{IRD4}	FO=4 Routing Delay			3.53	ns
t_{IRD8}	FO=8 Routing Delay			4.80	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO=32 FO=486		4.35 4.80	ns ns
t_{CKL}	Input HIGH to LOW	FO=32 FO=486		5.10 5.96	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32 FO=486	3.02 3.31		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO=32 FO=486	3.02 3.31		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=486		0.76 0.76	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=486	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=486	3.88 4.64		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32 FO=486	7.84 8.57		ns ns
f_{MAX}	Maximum Datapath Frequency	FO=32 FO=486		126.23 115.50	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Output Module Timing		**'–3 Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.40	ns
t_{DHL}	Data-to-Pad LOW		3.97	ns
t_{ENZH}	Enable Pad Z to HIGH		3.56	ns
t_{ENZL}	Enable Pad Z to LOW		3.94	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.20	ns
t_{ENLZ}	Enable Pad LOW to Z		6.71	ns
t_{GLH}	G-to-Pad HIGH		4.77	ns
t_{GHL}	G-to-Pad LOW		4.77	ns
t_{LSU}	I/O Latch Output Set-Up	0.67		ns
t_{LH}	I/O Latch Output Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.66	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.84	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		4.79	ns
t_{DHL}	Data-to-Pad LOW		3.51	ns
t_{ENZH}	Enable Pad Z to HIGH		3.56	ns
t_{ENZL}	Enable Pad Z to LOW		3.38	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.20	ns
t_{ENLZ}	Enable Pad LOW to Z		6.71	ns
t_{GLH}	G-to-Pad HIGH		6.83	ns
t_{GHL}	G-to-Pad LOW		6.83	ns
t_{LSU}	I/O Latch Set-Up	0.67		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.66	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.84	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.04	ns/pF

Notes:

1. Delays based on 35 pF loading.

A42MX36 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)

		Preliminary Information		
Logic Module Propagation Delays		**'–3 Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Combinatorial Functions				
t_{PD}	Internal Array Module Delay		1.31	ns
t_{PDD}	Internal Decode Module Delay		1.60	ns
Predicted Module Routing Delays				
t_{RD1}	FO=1 Routing Delay		0.94	ns
t_{RD2}	FO=2 Routing Delay		1.28	ns
t_{RD3}	FO=3 Routing Delay		1.61	ns
t_{RD4}	FO=4 Routing Delay		1.96	ns
t_{RD5}	FO=8 Routing Delay		3.31	ns
t_{RDD}	Decode-to-Output Routing Delay		0.34	ns
Sequential Timing Characteristics				
t_{CO}	Flip-Flop Clock-to-Output		1.29	ns
t_{GO}	Latch Gate-to-Output		1.29	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.32		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		1.56	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.68		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.31		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.35		ns

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Logic Module Timing		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations				
t_{RC}	Read Cycle Time	6.75		ns
t_{WC}	Write Cycle Time	6.75		ns
t_{RCKHL}	Clock HIGH/LOW Time	3.38		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		3.38	ns
t_{ADSU}	Address/Data Set-Up Time	1.62		ns
t_{ADH}	Address/Data Hold Time	0.00		ns
t_{RENSU}	Read Enable Set-Up	0.61		ns
t_{RENH}	Read Enable Hold	3.38		ns
t_{WENSU}	Write Enable Set-Up	2.70		ns
t_{WENH}	Write Enable Hold	0.00		ns
t_{BENS}	Block Enable Set-Up	2.77		ns
t_{BENH}	Block Enable Hold	0.00		ns
Asynchronous SRAM Operations				
t_{RPD}	Asynchronous Access Time		8.10	ns
t_{RDADV}	Read Address Valid	8.78		ns
t_{ADSU}	Address/Data Set-Up Time	1.62		ns
t_{ADH}	Address/Data Hold Time	0.00		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.61		ns
t_{RENHA}	Read Enable Hold	3.38		ns
t_{WENSU}	Write Enable Set-Up	2.70		ns
t_{WENH}	Write Enable Hold	0.00		ns
t_{DOH}	Data Out Hold Time		1.22	ns

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Advanced Information		
Input Module Propagation Delays			**'–3' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.03	ns
t_{INGO}	Input Latch Gate-to-Output[1]			1.40	ns
t_{INH}	Input Latch Hold[1]		0.00		ns
t_{INSU}	Input Latch Set-Up[1]		0.48		ns
t_{ILA}	Latch Active Pulse Width[1]		4.66		ns
Input Module Predicted Routing Delays					
t_{IRD1}	FO=1 Routing Delay			1.96	ns
t_{IRD2}	FO=2 Routing Delay			2.30	ns
t_{IRD3}	FO=3 Routing Delay			2.64	ns
t_{IRD4}	FO=4 Routing Delay			2.99	ns
t_{IRD8}	FO=8 Routing Delay			4.34	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO=32 FO=635		2.73 3.00	ns ns
t_{CKL}	Input HIGH to LOW	FO=32 FO=635		3.78 4.86	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32 FO=635	1.76 1.96		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO=32 FO=635	1.76 1.96		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		0.75 0.75	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=635	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	2.84 3.31		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32 FO=635	5.49 5.95		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		180.13 166.38	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Advanced Information		
Output Module Timing		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		2.56	ns
t_{DHL}	Data-to-Pad LOW		2.96	ns
t_{ENZH}	Enable Pad Z to HIGH		2.66	ns
t_{ENZL}	Enable Pad Z to LOW		2.93	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.26	ns
t_{ENLZ}	Enable Pad LOW to Z		4.91	ns
t_{GLH}	G-to-Pad HIGH		2.94	ns
t_{GHL}	G-to-Pad LOW		2.94	ns
t_{LSU}	I/O Latch Output Set-Up	0.48		ns
t_{LH}	I/O Latch Output Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.67	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.77	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.07	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.53	ns
t_{DHL}	Data-to-Pad LOW		2.46	ns
t_{ENZH}	Enable Pad Z to HIGH		2.66	ns
t_{ENZL}	Enable Pad Z to LOW		2.93	ns
t_{ENHZ}	Enable Pad HIGH to Z		5.26	ns
t_{ENLZ}	Enable Pad LOW to Z		4.91	ns
t_{GLH}	G-to-Pad HIGH		5.03	ns
t_{GHL}	G-to-Pad LOW		5.03	ns
t_{LSU}	I/O Latch Set-Up	0.48		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.67	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.77	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.07	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.07	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions, V_{CC} = 3.0V, T_J = 70°C)

		Preliminary Information		
Logic Module Propagation Delays		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Combinatorial Functions				
t_{PD}	Internal Array Module Delay		1.85	ns
t_{PDD}	Internal Decode Module Delay		2.24	ns
Predicted Module Routing Delays				
t_{RD1}	FO=1 Routing Delay		1.31	ns
t_{RD2}	FO=2 Routing Delay		1.78	ns
t_{RD3}	FO=3 Routing Delay		2.26	ns
t_{RD4}	FO=4 Routing Delay		2.75	ns
t_{RD5}	FO=8 Routing Delay		4.64	ns
t_{RDD}	Decode-to-Output Routing Delay		0.48	ns
Sequential Timing Characteristics				
t_{CO}	Flip-Flop Clock-to-Output		1.80	ns
t_{GO}	Latch Gate-to-Output		1.80	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.44		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.00		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.19	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.99		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.00		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.64		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.08		ns

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Logic Module Timing		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations				
t_{RC}	Read Cycle Time	9.45		ns
t_{WC}	Write Cycle Time	9.45		ns
t_{RCKHL}	Clock HIGH/LOW Time	4.77		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		4.77	ns
t_{ADSU}	Address/Data Set-Up Time	2.25		ns
t_{ADH}	Address/Data Hold Time	0.00		ns
t_{RENSU}	Read Enable Set-Up	0.90		ns
t_{RENH}	Read Enable Hold	4.77		ns
t_{WENSU}	Write Enable Set-Up	3.78		ns
t_{WENH}	Write Enable Hold	0.00		ns
t_{BENS}	Block Enable Set-Up	3.87		ns
t_{BENH}	Block Enable Hold	0.00		ns
Asynchronous SRAM Operations				
t_{RPD}	Asynchronous Access Time		11.34	ns
t_{RDADV}	Read Address Valid	12.33		ns
t_{ADSU}	Address/Data Set-Up Time	2.25		ns
t_{ADH}	Address/Data Hold Time	0.00		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.90		ns
t_{RENHA}	Read Enable Hold	4.77		ns
t_{WENSU}	Write Enable Set-Up	3.78		ns
t_{WENH}	Write Enable Hold	0.00		ns
t_{DOH}	Data Out Hold Time		1.80	ns

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information		
Input Module Propagation Delays			**'–3' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad-to-Y			1.44	ns
t_{INGO}	Input Latch Gate-to-Output[1]			1.95	ns
t_{INH}	Input Latch Hold[1]		0.00		ns
t_{INSU}	Input Latch Set-Up[1]		0.67		ns
t_{ILA}	Latch Active Pulse Width[1]		6.53		ns
Input Module Predicted Routing Delays					
t_{IRD1}	FO=1 Routing Delay			2.75	ns
t_{IRD2}	FO=2 Routing Delay			3.22	ns
t_{IRD3}	FO=3 Routing Delay			3.70	ns
t_{IRD4}	FO=4 Routing Delay			4.18	ns
t_{IRD8}	FO=8 Routing Delay			6.08	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO=32 FO=635		4.55 5.00	ns ns
t_{CKL}	Input HIGH to LOW	FO=32 FO=635		5.29 6.80	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32 FO=635	2.46 2.75		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO=32 FO=635	2.46 2.75		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.04 1.04	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=635	0.00 0.00		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.97 4.64		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32 FO=635	9.16 9.92		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		108.08 99.83	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Output Module Timing		**'–3' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		3.57	ns
t_{DHL}	Data-to-Pad LOW		4.15	ns
t_{ENZH}	Enable Pad Z to HIGH		3.72	ns
t_{ENZL}	Enable Pad Z to LOW		4.10	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.36	ns
t_{ENLZ}	Enable Pad LOW to Z		6.87	ns
t_{GLH}	G-to-Pad HIGH		4.91	ns
t_{GHL}	G-to-Pad LOW		4.91	ns
t_{LSU}	I/O Latch Output Set-Up	0.67		ns
t_{LH}	I/O Latch Output Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.94	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.87	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.10	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data-to-Pad HIGH		4.94	ns
t_{DHL}	Data-to-Pad LOW		3.44	ns
t_{ENZH}	Enable Pad Z to HIGH		3.72	ns
t_{ENZL}	Enable Pad Z to LOW		4.10	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.36	ns
t_{ENLZ}	Enable Pad LOW to Z		6.87	ns
t_{GLH}	G-to-Pad HIGH		7.04	ns
t_{GHL}	G-to-Pad LOW		7.04	ns
t_{LSU}	I/O Latch Set-Up	0.67		ns
t_{LH}	I/O Latch Hold	0.00		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.94	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.87	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.10	ns/pF

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

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