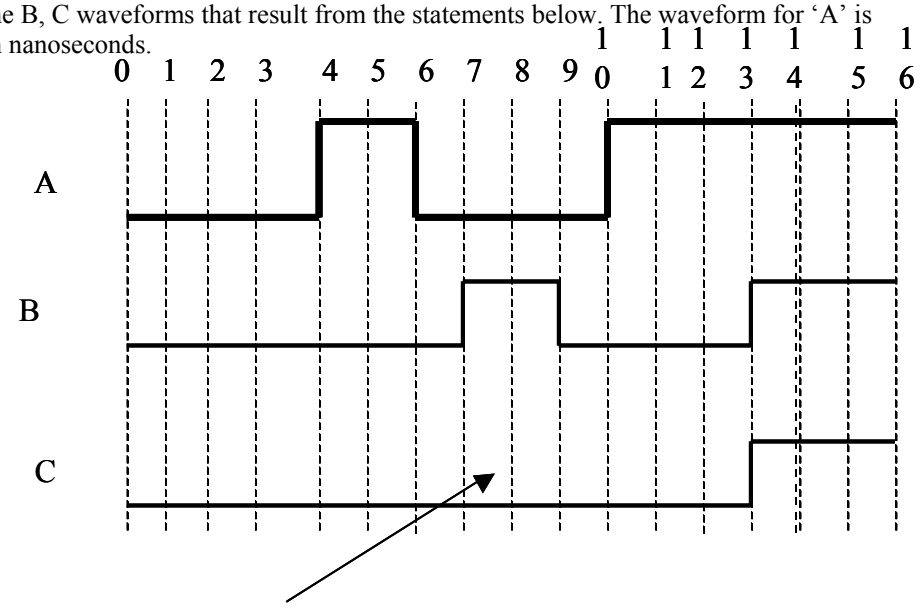
Spring 2003 – Test 1 Solution

1. (10 pts) Draw the B, C waveforms that result from the statements below. The waveform for 'A' is shown, time is in nanoseconds.



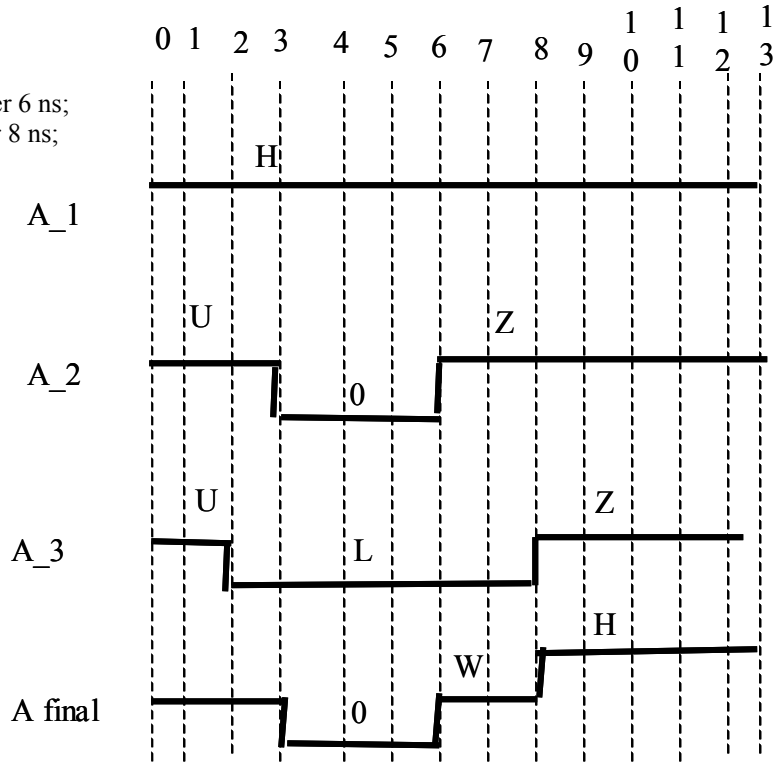
B <= transport 'A' after 3 ns;
C <= 'A" after 3 ns;

Inertial delay model rejects pulse.

2. (10 pts) Draw the waveform for A that results from the following statements (note that A has multiple drivers)

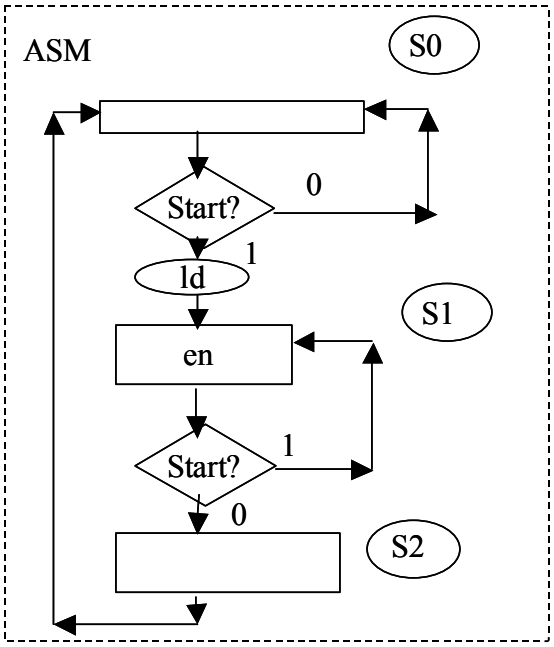
signal A: std_logic;

A <= 'H';
A <= transport '0' after 3 ns, 'Z' after 6 ns;
A <= transport 'L' after 2 ns, 'Z' after 8 ns;



3.

(20 pts) The code shown below implements the ASM chart. Modify this code so that an error message is printed if the finite state machines spends more than S1_MAX_CLOCKS consecutive clock cycles in state S1 at any time.




```
type mystate is (S0,S1,S2);
signal pstate,nstate: mystate;

process(clk)
 begin
  if (clk'event and clk = '1') then
     pstate <= nstate;
  end if;
 end process;

process(start, pstate'transaction)
variable cnt: integer := 0;

 begin
   ld <= '0'; en <= '0';
 case pstate is
  when S0 => if (start = '1') then
                ld <= '1';
               nstate <= S1;
               end if;
 when S1 =>
          if (pstate'active) then
            if (pstate'last_value = S1) then
                cnt := cnt + 1;
                assert (cnt < S1_MAX_CLOCKS)
                report "S1 Max clocks exceeded."
                severity error;
            else
                cnt := 1;
            end if;
          end if;
            en <= '1';
              if (start = '0') then
                  nstate <= S2;
              end if;
 when S2 => nstate <= S0;

end case;
```

trigger every clock

protect variable incrementation

reset the counter

4. (6 pts) Write or more or type definitions that can be used to define a memory of byte values; each byte is 8 bits, each bit is a std_logic type.

type bytemem is array (natural range <>) of std_logic_vector(7 downto 0);

OR

type byte is array (7 downto 0) of std_logic;
type bytemem is array (natural range <>) of byte;

5. (6 pts) Under what conditions is a resolved data type required?

when multiple drivers are required for a signal.

6. (6 pts) In a process with a sensitivity list, **show** how you can ensure that a statement (e.g. a FILE_OPEN) is executed a single time; with that execution taking place the first time the process is executed.

```
process (a_signal)
 variable init:Boolean;
 begin
 if (init = FALSE) then
      FILE_OPEN(….);
      init := TRUE:
end if;
….- -  rest of process
```

7. (6 pts) Give an example of when it might be useful for a VHDL model to read an input file at simulation time.

   A test bench often reads external test vectors from a file the provide signal values and times when they should be applied.

(6 pts) Give an example of when it might be useful for a VHDL model to read an input file at elaboration time.

The PLD example read the JEDEC file contents at elaboration time so that this could be used in GENERATE statements to produce a model with signals/process requirements that matched complexity of the logic in the PLD. A GENERATE block is expanded at elaboration time, so if this is to be parameterized by the contents of an external file, then the file must be read at elaboration time.

8. (6 pts) What can be controlled via a VHDL configuration?

   We controlled GENERIC values and ARCHITECTURE choices via configurations. A less common use is to specify a different entity for a component value – this only works if the port declarations are exactly the same between the two entities.

9. (6 pts) For any defined enumerated type, what is the default value?

The LEFTMOST value in the enumerated type.

10. (8 pts) Write a process that will track the maximum time separation between events on an input signal 'A'. After 1000 events, write this value to the standard output. The value must be reported as a time value.

```
 process (a)
 variable   max_time: time;
 variable cnt: integer:= 0;
 variable ll:line;
begin
 if (a'delayed'last_event > max_time) then
     max_time := a'delayed'last_event;
end if;
cnt: = cnt + 1;
if (cnt = 1000) then
  write(ll, string'("Max event delta is:"));
  write(ll,max_time);
  writeline(OUTPUT,ll);
end if;

end process;
```

11. (8 pts) Show how you would define a type in VHDL that can be dynamically allocated at run time. Use a record type as an example that could be used to form a linked list. Show how a variable of this type would be allocated.

```
 type   myrecptr is access myrec;   -- pointer must be access type.
type myrec is
   record
      a_int:  integer;
      a_ptr: myrecptr;
   end record myrec;

 variable a_rec: myrec;

 a_rec :=  new  myrec;          -- 'new' used for dynamic allocation of value.
```

13. (4 pts) What is the '-' (a dash) value in the std_logic type mean and when is it useful?

It is a don't care value and it is primarily used for logic synthesis. It is typically never assigned for simulation purposes.