Comments on: A robust single phase clocking for low power, high-speed VLSI applications

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ABSTRACT

Some of the material in a recent paper by Afghahi[1] has been previously published. A divide-by-two circuit described therein is clock edge-sensitive rather than frequency dependent, and cannot be understood in terms of connecting two digital latches.

In a recent paper[1], Afghahi presented several latch and flip-flop designs. Two of the main flip-flops presented ([1], Figs 3a and 9b) can also be found in the second edition of the text book by Weste and Eshraghian[2]; the only difference is the order of the *clk* and *data* transistors which does not alter the logical operation. As Weste and Eshraghian point out (but Afghahi does not) these flip-flops require careful design: ratioing of the p- and n-type transistors is necessary for correct operation. For completeness, we note that another flip-flop with many advantages similar to the ones described by Afghahi has been reported by Matsui *et al*[3].

Afghahi also derives a simplified latch and flip-flop structure ([1] Figs 5b and 6). Fig. 1. shows the simplified Nlatch (with cross-coupled p-types); the flip-flop is formed by cascading this with the corresponding Platch (with cross-coupled n-types). To demonstrate the operation of the flip-flop, Afghahi connected the outputs of the flip-flop to the inverse inputs to form a divide-by-two circuit (as redrawn in Fig. 2) which is said to function with a clock in the 1MHz to 1GHz frequency range. To repeat these findings, we simulated the circuit in HSPICE using level 6 parameters from a 1u CMOS technology (ECPD10 from ES2-ATMEL). Using parameters for *typical* industrial conditions, minimum-sized transistors (w=1.2u, l=1.0u) and a 10MHz clock; the simulation results are shown in Fig. 3.

To understand the operation, consider Fig. 2. When *clk* is *high,* x and q are connected to form an inverter which is cross-coupled with an inverter formed by the connection of $\bar{x}$ and $\bar{q}$. When *clk* is *low,* x is connected instead to $\bar{q}$, and $\bar{x}$ to q. As the clock changes, the charge and transistor states established at the four nodes during the previous clock phase (and inverter pairs) are mixed; the new cross-coupled inverters then fall into a state which depends upon the relative voltage levels in their inputs.

Factors which effect these levels include the threshold voltage drop which occurs on each drain-node at some time through the circuit's cycle as shown in Fig. 3; this allows an essentially two state system to exhibit four states. When the new pairings of transistors form inverters, one of the four drains has an initial voltage level a threshold below that of the corresponding transistor in the other inverter; and this may determine the next state.

However, other factors can override this by causing in imbalance of charge and/or current including: mismatched drive strengths of the p- and n-type transistors, and unequal capacitances on the transistor drains. Parasitic coupling capacitance of a particular layout may also contribute to an imbalance and all these factors are susceptible to process variation.

The circuit is not frequency dependent (as stated by Afghahi) but rather clock-edge dependent; his use of a sine wave input, with faster edges for higher frequencies, may be the reason for this error. This can be seen in Fig. 3. where the voltage levels are constant between clock transitions. If the edge is too slow (> ~15nsec), then the charge on the drains of all four cross-coupled transistors is well mixed and the factors other than the threshold voltage drop will consistently dominate the outcome (thus causing the circuit to follow the clock).

In summary, while the circuit is fascinating, it is not sufficient to describe it in terms of the combination of digital latches: its operation depends upon charge sharing and a threshold-voltage drop. The circuit is clock-edge sensitive, does not function with consistently-full voltage levels on the outputs (which would assist in low-power system design), and requires careful transistor ratioing and circuit layout to achieve correct operation with robustness to process variation.

References

1. M Afghahi, “A robust single phase clocking for low power, high-speed VLSI applications”, *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 247-254, Feb 1996.
2. N Weste and K Eshraghian, *Principles of CMOS VLSI Design - A Systems Perspective,* Addison-Wesley, 1993 (2nd edition). Page 328
3. M Matsui, Y Uetani, L Kim, T Nagamatsu, Y Watanabe, A Chiba, K Matsuda, and T Sakuri, “A 200 MHz 13 mm-sq 2-D DCT Macrocell Using Sense-Amplifying Pipeline Flip-Flop Scheme”, *IEEE Journal of Solid State Circuits*, vol. 29, pp. 1482-1490, Dec 1994.

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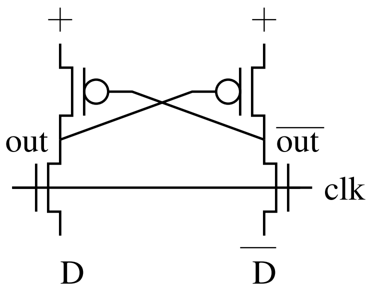

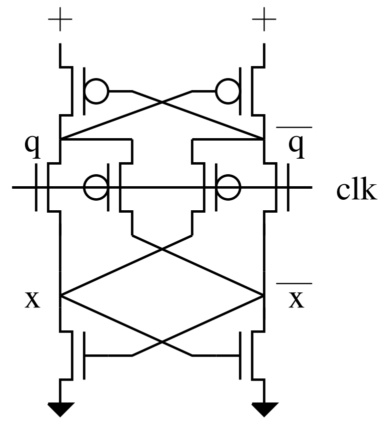

Fig. 1. Simplified N-latch from [1]

Fig. 2. (Redrawn) divide-by-two circuit from [1]

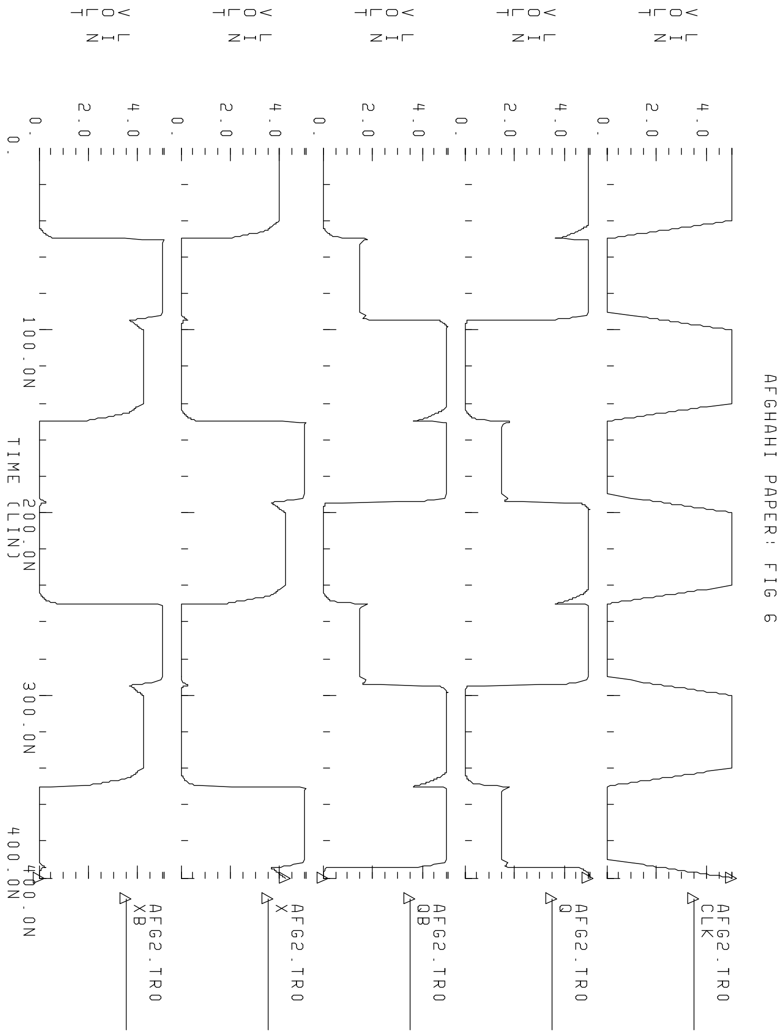

Fig. 3. Simulation of divide-by-two circuit