Silicore Corporation

Datasheet For The:

Silicore SLC1657 8-BIT RISC Microcontroller / VHDL Core

Overview

The Silicore SLC1657 is an eight-bit RISC microcontroller. It is delivered as a VHDL soft core module, and is intended for use in both FPGA and ASIC type devices. It is useful for microprocessor based embedded control applications such as: sensors, medical devices, consumer electronics, automotive systems, telecommunications, military and industrial controls.

The core is especially useful wherever there is limited printed circuit board space. All microprocessor and application functions can be integrated onto a single FPGA or ASIC device, thereby creating a very compact design. For example, very small sensor circuits can be created with this core.

When implemented on an FPGA device, the SLC1657 offers a completely user-defined microcontroller. This eliminates expensive NRE charges and lengthy lead times which are common for semi-custom integrated circuits. The end user can completely control the entire system integration process.

The core is also useful for high volume applications. That's because it is unusually compact, and can be produced inexpensively in ASIC parts.

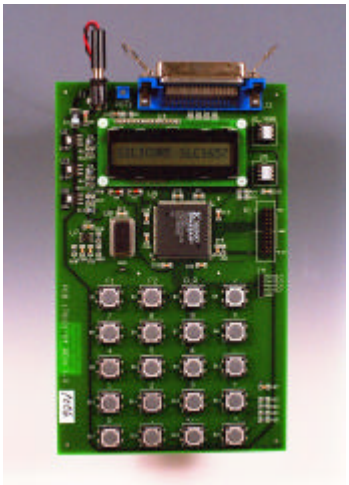
The SLC1657 can be used in a number of FPGA and ASIC target devices. This gives the user a wide range of options in mechanical packaging and temperature ranges.

Numerous software tools are available for the SLC1657. The core is software compatible with the industry standard PIC® series of microcontrollers made by Microchip Technology Inc. There are also many software tools available from third-party vendors. These include assemblers, 'C' compilers, simulators and fuzzy logic tools.

The core is delivered as soft IP (software) under the GNU Lesser GPL (LGPL) license from the Free Software Foundation (Boston, MA). The core can be used and modified in accordance with the LGPL without any royalty or other financial obligation to Silicore Corporation. It includes all VHDL source code, test benches and technical reference manuals. Factory technical support, system integration, evaluation boards and training are also available from Silicore Corporation at an additional charge.

The SLC1657 evaluation boards demonstrate the capabilities of the microcontroller. These are available with Agere, Altera or Xilinx FPGA parts. The boards demon-

strate how the microcontroller works in a variety of ways. The board shown below configures the SLC1657 as a four-function calculator. It also allows the user to assemble, download and run their own application software through a PC compatible parallel port cable.



SLC1657 Evaluation Board.

SLC1657 Features

- Eight-bit RISC microcontroller.
- Dual instruction and data buses with Harvard architecture.
- Fast operation...all microcontroller instructions (except branches) require one clock cycle. Branch instructions require two clock cycles.
- Very compact design minimizes gate count.
- 24 input and 48 output I/O lines.
- General purpose, eight-bit timer/counter module.
- Power-down/sleep mode for low power applications.
- Instruction ROM: up to 2,048 x 12 bit. Can be configured as embedded ROM, as an emulation ROM for software development purposes, or both.
- General purpose registers (RAM): up to 72 bytes.
- 32 op-code instructions with easy-to-use application software environment.
- A large base of software, tools and reference books are available.
- Microcontroller design written in the flexible VHDL hardware description language. The SLC1657 is delivered as a soft core, meaning that all VHDL source code and test benches are supplied. This allows the user to tweak the design for a particular application. Complete documentation is also provided.
- Very portable design can be operated on a wide variety of FPGA and ASIC target devices.
- Straightforward synchronous design simplifies system integration.
- Very simple timing constraint definition.
- The maximum operating speed is a function of the target device technology[1].

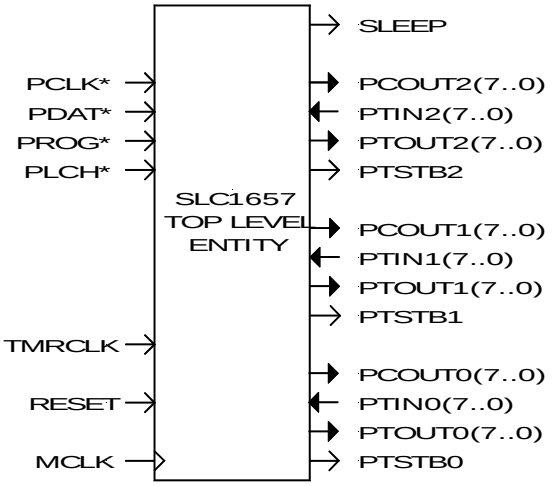
External Architecture

The core has a classic microcontroller topology. Connections are quite simple and include clock, reset, timer/counter input, sleep pin and I/O ports. An optional emulation ROM capability can also be used. This

[1] For example, the design operates on a Xilinx Spartan 2 FPGA at about 20 MHz (20 MIPS).

allows instructions to be downloaded through a PC compatible parallel port.

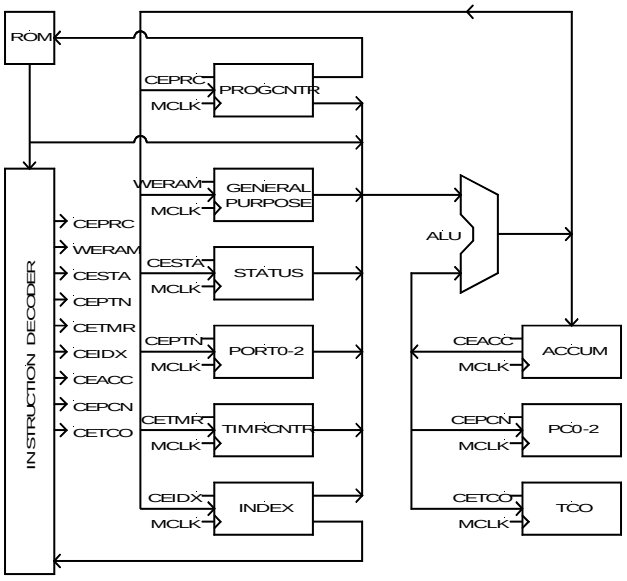
All I/O is handled through 24 input lines and 48 output lines. These can be used independently, or can be configured as three bi-directional ports (buses). Each port has an output strobe for connection to external FIFO buffers.



VHDL Top Level Entity Description

Internal Architecture

The SLC1657 uses a classic Harvard architecture. This means that it has dual instruction and data buses, and an unencoded instruction stream. This creates both a fast processor, and a very simple design topology. Furthermore, the design is completely synchronous. All operations occur at the rising edge of MCLK. This makes the design portable across many FPGA and ASIC target devices.



Internal Architecture

Signal Name	I/O Type	Signal Description
MCLK	I	Microcontroller clock
PCLK*	I	Program clock (EMR)
PCOUT0-2(7..0)	O	Port control output
PDAT*	I	Program data (EMR)
PLCH*	I	Program latch (EMR)
PROG*	I	Program enable (EMR)
PTIN0-2(7..0)	I	I/O PORT input
PTOUT0-2(7..0)	O	I/O PORT output
PTSTB0-2	O	Port output strobe
RESET	I	Reset (external)
SLEEP	O	Sleep mode
TMRCLK	I	External timer clock

EMR: Optional Emulation ROM.

Signal Description

Register	Address	R/W Access
ACCUM	Implicit	R/W
PC0	Implicit	W
PC1	Implicit	W
PC2	Implicit	W
TCO	Implicit	W
STACK1	Implicit	R/W
STACK2	Implicit	R/W
INDIRECT	0x00	R/W
TIMRCNTR	0x01	R/W
PROGCNTR	0x02	R/W
STATUS	0x03	R/W
INDEX	0x04	R/W
PORT0	0x05	R/W
PORT1	0x06	R/W
PORT2	0x07	R/W
GEN PURPOSE	0x08 - 0x7F	R/W

Internal Register Set

Instruction Set

The core is controlled by a simple instruction set with a total of 32 op-codes. These include add, subtract, increment, decrement, logical, loop and branch instructions. A branch-to-subroutine and a small (two level) stack is also included.

VHDL Synthesis & Tools

The SLC1657 is delivered as VHDL source code. The core must be synthesized by the user before operation on a particular target device (such as an FPGA or ASIC). Most of the internal entities are provided with the source code. However, there are a few exceptions. RAM, ROM and I/O drivers must be synthesized with entities provided by the FPGA or ASIC vendor. That's because portable, sythesizable RAM and ROM elements are not supported by the VHDL standards. Examples of complete design solutions are provided in the SLC1657 Technical Reference Manual.

The SLC1657 is provided as a soft core. This means that all VHDL source code and test benches are provided with the design.

It is assumed by Silicore Corporation that all simulation and synthesis tools conform to the following standards: IEEE STD 1076 1993, IEEE STD 1073.3-1997 and IEEE STD 1164-1993.

Almost any synthesis tool that supports common VHDL structures can be used. The original core was created with the Altium Accolade PeakFPGA synthesis and simulation tool.

Evaluation Boards

Several evaluation boards are available for the SLC1657. These allow the user to demonstrate and evaluate the microcontroller. Specific features of the boards include:

- Agere ORCA 3L, Altera FLEX 10KE or Xilinx Spartan 2.
- Demonstration and 4-function calculator ROMs.
- PC download cable
- PC download software
- 5 MHz / 5 MIPS crystal clock oscillator.
- 9 VDC battery pack.
- 16 x 1 LCD module.
- 16 keyswitches.
- 1 KHz free running oscillator.
- Complete instructions and technical reference manual.

Mnemonic	Operand	Description		Mnemonic	Oper-and	Description
ADD	R,D	ADD register and ACCUM		MOVI	V	Move immediate to ACCUM
AND	R,D	AND register with ACCUM		MOVP	-	Move ACCUM to PC0-2
ANDI	V	AND immediate with ACCUM		MOVT	-	Move ACCUM to TCO
BCLR	R,B	Clear register bit		NOP	-	No operation
BRA	V	Branch		NOT	R,D	NOT register
BSET	R,B	Set register bit		OR	R,D	OR register with ACCUM
BSR	V	Branch to subroutine		ORI	V	OR immediate with ACCUM
BTSC	R,B	Test bit and skip if clear		PWRDN	-	Power-down
BTSS	R,B	Test bit and skip if set		RET	V	Return from subroutine
CLR	R,D	Clear register or ACCUM		ROL	R,D	Rotate register left
DEC	R,D	Decrement register		ROR	R,D	Rotate register right
DECSZ	R,D	Dec. register, skip if zero		RWT	-	Reset watchdog timer
INC	R,D	Increment register		SUB	R,D	Subtract ACCUM from register
INCSZ	R,D	Inc. register, skip if zero		SWPN	R,D	Swap nibbles in register
MOV	R,D	Move register		XOR	R,D	XOR register with ACCUM
MOVA	R	Move ACCUM to register		XORI	V	XOR immediate with ACCUM

Instruction Set Summary

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