0.25 µm FLASH Memory Based FPGA for Space Applications

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Abstract

The potential of a FLASH memory based FPGA, ProASIC, is investigated for space applications. The configuration cell is using a state-of-art 0.25µm FLASH technology. The technology and architecture are introduced. The manifestation of total dose and single event effects is discussed.

I. Introduction

In 1998, Actel entered into a partnership with Gatefield Corporation. In the partnership, Actel will market and sell the ProASIC line of 0.25 µm FLASH based FPGAs that were designed by Gatefield. The ProASIC FPGAs are manufactured with a state-of-the-art FLASH process by Infineon (formerly Siemens).

FPGA products based on a one-time programmable (OTP) anti-fuse switch element are used almost exclusively for space applications. The challenge for a reprogrammable FPGA suitable for space applications is primarily the SEU tolerance of the switch element. Referring to Figure 1, a 10,000 gate FPGA with 240,000 switch elements, each with an upset rate of 10^{-7} upset/bit-day (typical for an SRAM cell in a LEO orbit), will experience a functional failure every 1000 hours. The problem is compounded as design complexity increases or upset rate increases in more severe environments.

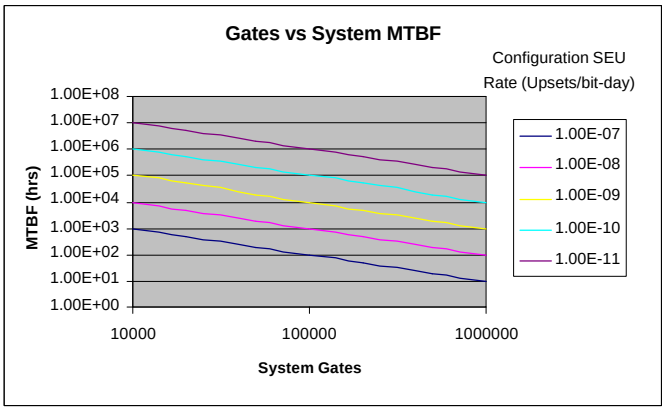

Figure 1. Plot of mean time between failure (MTBF) as a function of system gate count for several switch element upset rates. The lower line corresponds to an upset rate of 1.0e-7.

Based on theoretical and experimental work with FLASH memory cells, an FPGA based on a FLASH switch-element has the promise of offering reprogrammability without sacrificing much of the desirable characteristics of an anti-fuse, namely non-volatility, as does an SRAM based FPGA.

The purpose of this paper is to introduce the technical capabilities of the ProASIC architecture and to discuss issues with the performance of the ProASIC FPGA in a space environment.

II. DISCUSSION

A. Technology

The switch (Figure 2) consists of two devices. One is a smaller, minimum geometry device, used for programming the switch. The second, larger device, is a pass transistor switch element used to connect or disconnect two nodes in the FPGA.

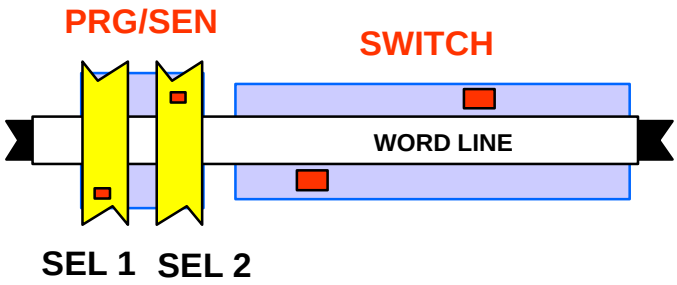

Figure 2. Top level view of the FLASH based FPGA switch.

Electrically, the floating gate is shared by both the programming and the switch transistors (Figure 3). The control gate is also shared.

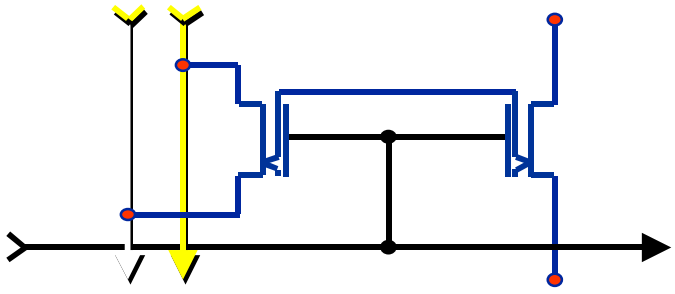

Figure 3. Schematic view of the FLASH based FPGA switch. The programming device in on the left and the switching device is on the right.

Programming is accomplished with Fowler-Nordheim tunneling. A switch is turned on by ramping the control gate to –11.0 volts while holding the source and drain of the programming transistor at 5.0 volts. In normal operation, the

control gate is held at 2.5 volts (V_{CC}). The charge on the floating gate couples with the control gate to achieve an effective gate voltage that is approximately 4.5 volts.

Erasing is also accomplished with Fowler-Nordheim tunneling. A switch is turned off by holding the source and drain of the programming transistor at ground while ramping the control gate to 16.0 volts. The net result during normal operation is that the floating gate on the switch is less than 0 volts.

The bottom gate oxide is approximately 8.5 nm. There is an additional implant in the drain region of the programming device to enhance the tunneling current. The top gate oxide is approximately 18 nm of ONO.

A major benefit of the FLASH technology in space applications is the lower power consumption that is a direct result of the FLASH switch. A single transistor programming element (vs. 5 for an SRAM switch) results directly in a smaller die size. Since FPGA power consumption is dominated by interconnect, the smaller die size translates to less power. For example, an FIR filter implemented in a FLASH based consumes one third the power as it does when implemented in a comparably sized SRAM based FPGA (Figure 4).

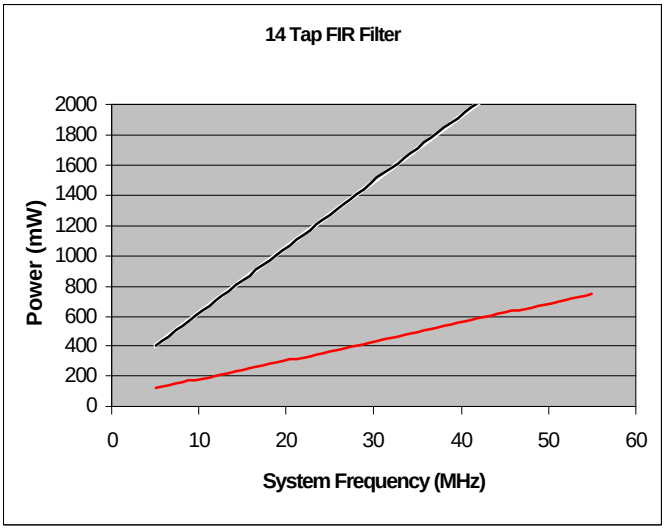

Figure 4. Comparison of power consumption between the FLASH based FPGA (lower line) and a functionally equivalent SRAM based FPGA (upper line)

B. Architecture

Like all FPGA architectures, the FLASH based ProASIC device consists of an array of logic cells and a ring of I/O elements. In addition, flexible 256x9 blocks of SRAM are arranged at the top of the array (Figure 5.).

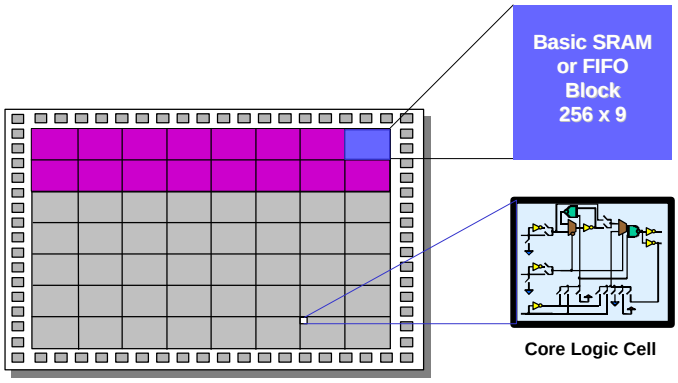

Figure 5. Layout of the FLASH based FPGA array.

1) *Logic Tile*

The logic tile (Figure 6.) can implement either a flip-flop with a set/reset pin or a 3-input combinatorial function. The functionality is configured by programming the appropriate switching elements. The combinatorial function utilizes the 2-input multiplexer in the slave portion of the flip-flop. This structure can implement 44 unique logic functions, including all possible 2-input functions. It cannot implement a 3-input XOR and is therefore less than optimal for high performance arithmetic operations.

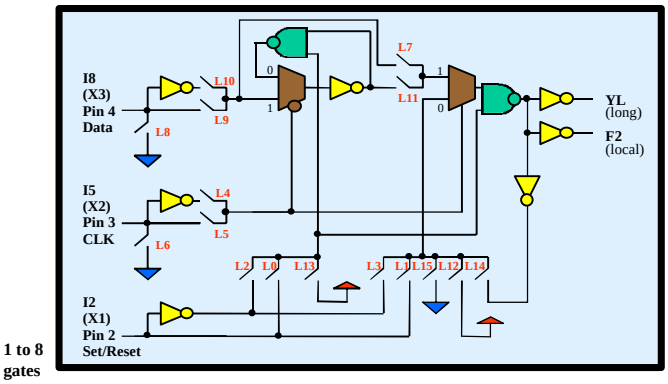

Figure 6. ProASIC logic tile.

One relatively unique aspect of this architecture is that, unlike most FPGAs, registers are relatively low cost. In other words, a register can be used without losing the capability of other combinatorial logic in the basic logic element. This is beneficial in most implementations of high performance DSP data-paths where large numbers of registers are needed to store the sampled data. It also is helpful if triple modular redundancy (TMR) is needed for SEU mitigation.

2) *Routing Resources*

There are 4 distinct classes of routing resources in the architecture (Figure 7.) There are 4 global networks used for clocks and global control signals such as set/reset or enables. Abundant high speed bus lines run the length and width of the chip and yield corner to corner delay of less than 4 ns. Efficient long lines are used to rout signals up to 4 tiles long

and ultra-fast local lines rout signals from one tile to 8 adjacent tiles in less than 0.5 ns.

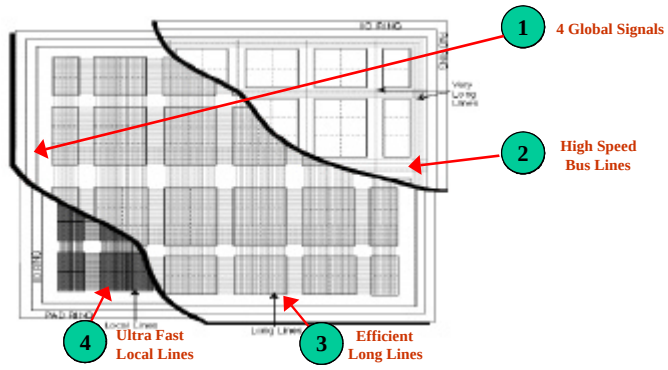

Figure 7. Routing resources.

A novel feature of the global resources (Figure 8.) is that unused spines in the H-tree distribution are turned off, resulting in significant power savings.

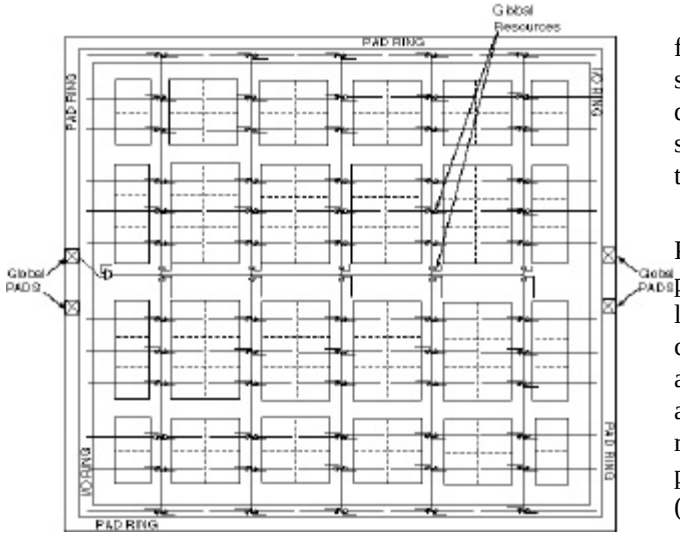

Figure 8. Global routing resources.

3) *I/O*

The I/O can be selected (Figure 9), on an individual basis, to drive either 3.3 volts or 2.5 volts. At 3.3 volts, the I/O drive meets the requirements for 3.3 volts PCI. The logic core must be powered with 2.5 volts V_{CC}.

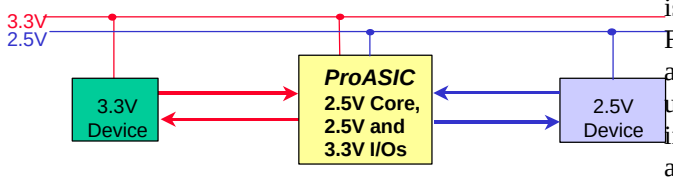

Figure 9. I/O block interfacing.

C. *Radiation Effects*

1) *Switch SEU*

Unlike an SRAM switch, a FLASH switch is intrinsically hard. The upset mechanism is for a heavy ion to discharge the floating gate by generating charge in the bottom and top oxides that diffuse to the floating gate. Calculations show that, for the ProASIC switch, the amount of charge generated by an ion with LET of 37 MeV-cm^2/mg is less than 1% of the total charge on a programmed floating gate.

This theoretical assessment of SEU hardness is backed by experimental results showing the memory cell of a Hitachi 1Mbit EEPROM with a LET_{th} exceeding 37 MeV-cm^2/mg [1].

2) *Total Ionizing Dose (TID)*

TID effects are expected to be the worst case combined effects of 0.25 µm CMOS performance and 0.25 µm FLASH performance. Data (for example, see [2]) suggests that the CMOS process at 0.25 µm will be hard to at least 50 krad(Si).

Previous test results make it unclear as to what to expect for the FLASH component of the process. There is data showing poor TID performance of commercial FLASH devices. However, failure often occurs in the peripheral support circuits such as the charge pump and is not a result of the performance of the FLASH cell itself [3].

The ProASIC FPGA does not have a charge pump. Programming voltages are supplied externally. This is possible because, most FPGA applications will have a very low programming duty cycle. Usually, it is only necessary to configure the device during prototyping. Once the application is fielded or launched, it will not be programmed again. There are certain applications that do require field reprogrammability. These range from infrequent programming (field updates) to frequent programming (reconfigurable computing).

Dissipation of the charge on the floating gate due to TID effects may also be of concern in a FLASH process. If this effect is significant, it could be potentially mitigated by periodically refreshing the memory cells in the array. As stated, programming voltages will need to be supplied externally for such an application.

3) *Single Event Latch-up*

Latch-up is a design dependent phenomenon more that it is a process dependent phenomenon. As FLASH based FPGA was designed for the commercial market, special attention was not paid to latch-up mitigation. Given the uncertainty of the expected result, latch-up testing is highest in priority. If the results prove to be unacceptable for space applications, the first level of mitigation will be to use epi wafers.

One area of special concern regarding latch-up is during programming of the device. During normal operation, 3.3 volts is the highest supply potential. During programming, the voltage can be as high as 16 volts. It is during

programming that many of the high voltage circuits, used only for programming, will be vulnerable to latch-up. Again, it is expected that most applications will not require in field reprogrammability so this issue may not be of concern. However, it does make the suggested mitigation technique for floating gate dissipation less attractive.

4) Single Event Gate Rupture (SEGR)

SEGR is not expected to be a concern during normal operation. However, during programming, the part will be vulnerable to this phenomenon when there is a 16 volt potential difference between the gate region of the FLASH device and the control gate.

5) Flip-flop SEU

The SEU performance of the user flip-flops is expected to be no better or worse than the SEU performance of 0.25 µm CMOS flip-flops in other FPGA technologies. Inspection of the logic tile (Figure 3.) does show that there is a switch in the feedback path of the slave latch portion of the flip flop. This switch will have the effect of adding resistance to the path and may enhance SEU performance of the slave latch. If this is the case, there will be a duty cycle dependence for SEU which can be easily observed.

6) Single Event Transients (SET)

Single event transient occurs when a heavy ion hits on a circuit node and induces a pulse or a glitch. It is a phenomenon that is present in all CMOS ASIC devices and can lead to soft-errors in the flip-flop when the transient pulses arrive during the set-up and hold window of the flip-flop.

In SRAM FPGAs, SETs can occur in the configuration memory, temporarily switch the pass-transistor into an undesired state and cause error signals passing through the data paths.

The FLASH FPGA storage element is not expected to be sensitive to SET. As mentioned in subsection II C 1), the amount of charge induced by an ion hit is very small relative to the storage charge on the floating gate.

7) Summary of Radiation Effects.

	0.25um FLASH	**0.25um SRAM**
SEU	Data Error	Data Error + Functional Interrupt
SET	CMOS	CMOS + Configuration Bits
SEL	CMOS	CMOS
SEDR	Only during Programming	No
TID	> 50krad(Si)	> 50krad(Si)

Figure 10. Comparison of radiation effects between a FLASH based and SRAM based FPGA.

Figure 10 contrasts the expected radiation performance of a FLASH based reconfigurable FPGA with an SRAM based reconfigurable FPGA. The FLASH based FPGA is expected to be clearly superior in terms of configuration SEU and therefore mitigate the functional upset concerns illustrated in Figure 1.

The SRAM FPGA may be superior for in orbit reconfiguration applications, depending on the severity of the radiation effects observed during programming of the FLASH FPGA.

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