HiRel SX-A Family FPGAs

Leading Edge Performance

- 215 MHz System Performance (Military Temperature)
- 5.3 ns Clock-to-Out (Pin-to-Pin) (Military Temperature)
- 240 MHz Internal Performance (Military Temperature)

Specifications

- 48,000 to 108,000 Available System Gates
- Up to 228 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.25/0.22µ CMOS Process Technology

Features

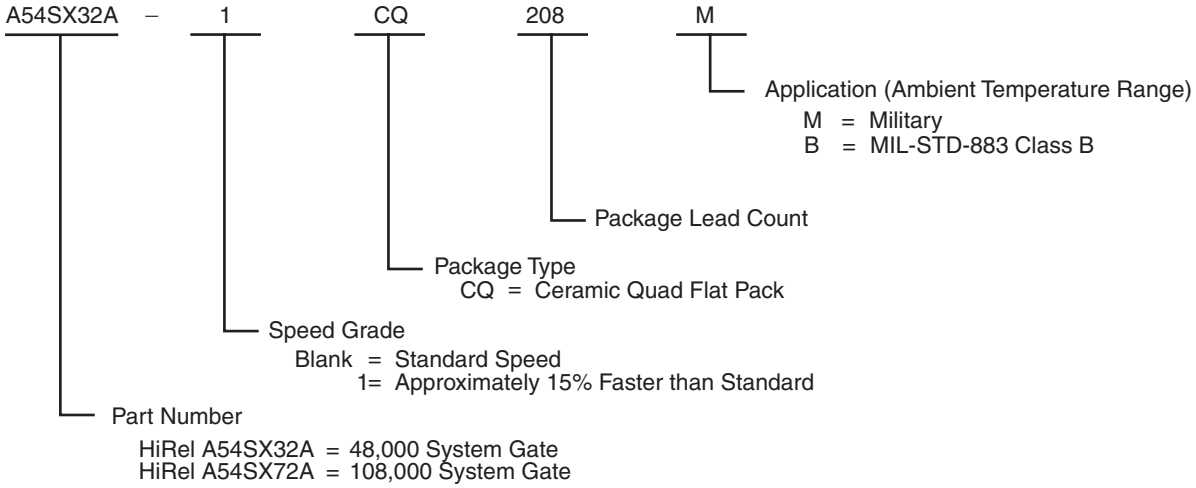
- I/Os with Live or "Hot-Swapping" Capability
- Power-Up/Down Friendly
- Standard Hermetic Package Offerings
- Class B level Devices
- Two Hermetic Package Options
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Cold-Sparing Capability
- Slow Slew Rate Option
- QML Certified Devices
- 100% Military Temperature Tested (–55°C and +125°C)
- 33 MHz PCI Compliant
- CPLD and FPGA Integration
- Single-Chip Solution
- Configurable I/O Support for 3.3V/5V PCI, LVTTL, and TTL
- Configurable Weak Resistor Pull Up or Pull Down for Tristated Outputs during Power Up
- 100% Resource Utilization with 100% Pin Locking
- 2.5V, 3.3V, and 5V Mixed Voltage Operation with 5V Input Tolerance and 5V Drive Strength
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)

Product Profile

Device	HiRel A54SX32A	HiRel A54SX72A
Capacity		
Typical Gates	32,000	72,000
System Gates	48,000	108,000
Logic Modules	2,880	6,036
Combinatorial Cells	1,800	4,024
Register Cells		
Dedicated Flip-Flops	1,080	2,012
Maximum Flip-Flops	1,980	4,024
Maximum User I/Os	228	213
Global Clocks	3	3
Quadrant Clocks	0	4
Boundary Scan Testing	Yes	Yes
3.3V/5V PCI	Yes	Yes
Clock-to-Out	5.3 ns	6.7 ns
Input Set-Up (External)	0 ns	0 ns
Speed Grades	Std, –1	Std, –1
Package (by pin count)		
CQFP	208, 256	208, 256

**See Actel's website for the latest version of the datasheet. This datasheet is web-only.*

Ordering Information



Product Plan

	Speed Grade*		Application	
	Std	–1	M	B
HiRel A54SX32A Device				
208-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
256-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
HiRel A54SX72A Device				
208-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
256-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔

Contact your Actel sales representative for product availability.

Applications: M = Military Temp
B = MIL-STD-883 Class B

Availability: ✔ = Available

**Speed Grade: –1 = Approx. 15% faster than Standard*

Ceramic Device Resources

Device	User I/Os (including clock buffers)	
	CQFP 208-Pin	CQFP 256-Pin
HiRel A54SX32A	174	228
HiRel A54SX72A	171	213

Package Definitions

CQFP = Ceramic Quad Flat Pack

Actel MIL-STD-883 Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Test Condition D, Y_1, Orientation Only	100%
4.	Seal a. Fine b. Gross	1014	 100% 100%
5.	Visual Inspection	2009	100%
6.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
7.	Burn-in Test	1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C	100%
8.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
9.	Percent Defective Allowable	5%	All Lots
10.	Final Electrical Test a. Static Tests (1) 25°C (Subgroup 1, Table I) (2) –55°C and +125°C (Subgroups 2, 3, Table I) b. Functional Tests (1) 25°C (Subgroup 7, Table I) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I) c. Switching Tests at 25°C (Subgroup 9, Table I)	In accordance with applicable Actel device specification, which includes a, b, and c: 5005 5005 5005 5005 5005	 100% 100% 100%
11.	External Visual	2009	100%

General Description

Actel's HiRel versions of the SX-A Family of FPGAs offer advantages for applications such as commercial and all types of military and high reliability equipment.

The HiRel versions are fully pin compatible allowing designs to migrate across different applications that do not have radiation requirements. Additionally, the HiRel devices can be used as a lower cost prototyping tool for RT designs. This datasheet discusses HiRel SX-A products. Refer to Actel's web site for more information concerning RadTolerant products.

The programmable architecture of these devices offer high performance, design flexibility, and fast and inexpensive prototyping – all without the expense of test vectors, NRE charges, long lead times, and schedule and cost penalties for design modifications that are required by ASIC devices.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military, and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable, and cost-effective logistics support throughout QML products' life cycles.

HiRel SX-A Family Architecture

The HiRel SX-A family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

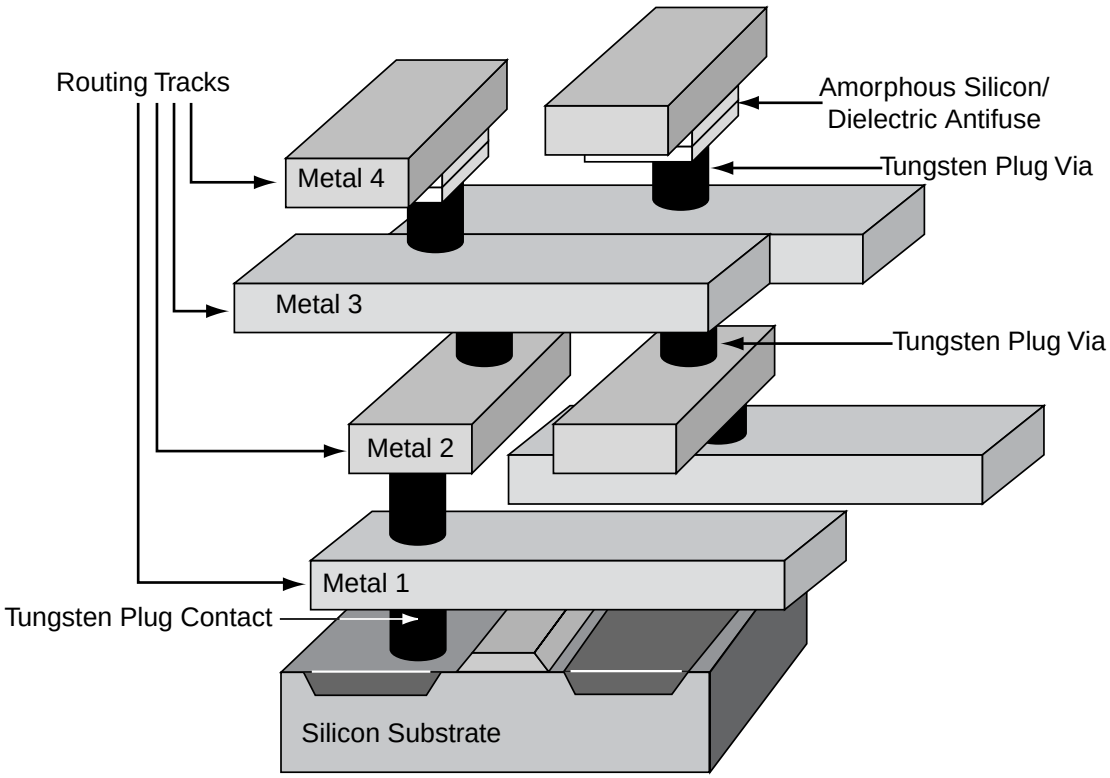
Programmable Interconnect Element

The HiRel SX-A family incorporates either three (in HiRel A54SX32A) or four (in HiRel A54SX72A) layers of metal interconnect and provides efficient use of silicon by locating the routing interconnect resources between the top two metal layers (Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs) and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded in the top two layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the HiRel SX-A family abundant routing resources and provides excellent protection against design theft. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. Additionally, since HiRel SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept.

The HiRel SX-A interconnect (i.e., the antifuses and metal tracks) also has lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry for the radiation tolerance offered.



Note: *HiRel A54SX72A has four layers of metal with the antifuse between Metal 3 and Metal 4. HiRel A54SX32A has three layers of metal with antifuse between Metal 2 and Metal 3.*

Figure 1 • *HiRel SX-A Family Interconnect Elements*

Logic Module Design

The HiRel SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's HiRel SX-A family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the HiRel SX-A FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock, the routed clocks, or the internal logic.

The C-cell implements a range of combinatorial functions up to 5 inputs (Figure 3). Inclusion of the DB input and its associated inverter function increases the number of combinatorial functions that can be implemented in a single module from 800 options (as in previous architectures) to more than 4,000 in the HiRel SX-A architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

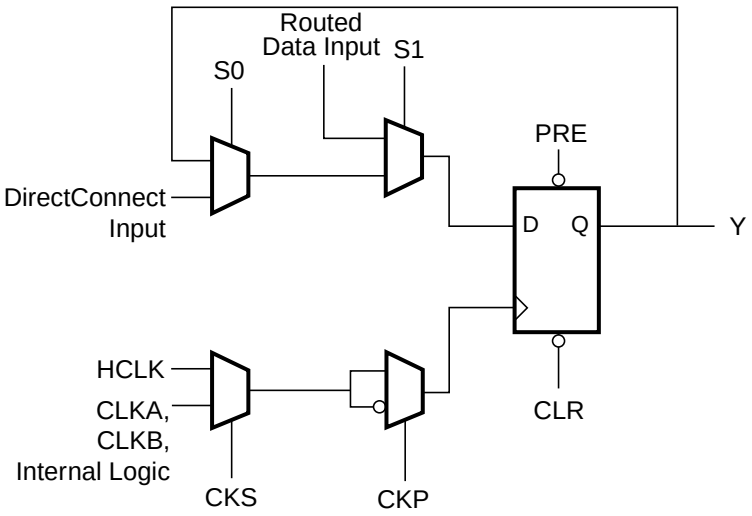


Figure 2 • R-Cell

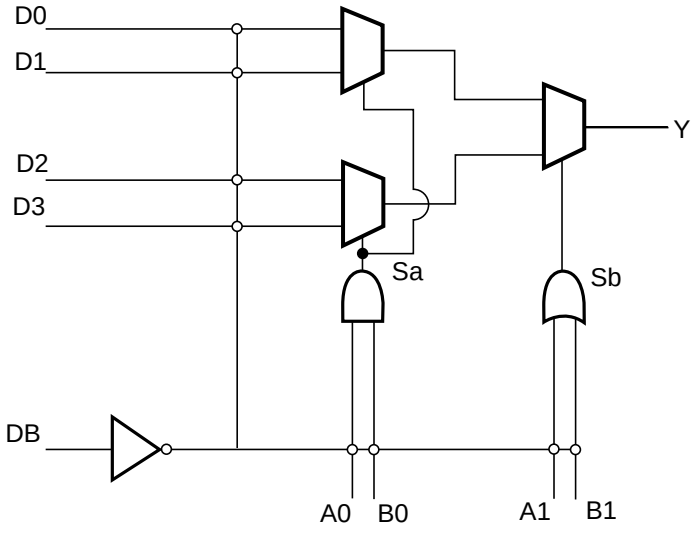


Figure 3 • C-Cell

Chip Architecture

The HiRel SX-A family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 clusters contain two C-cells and one R-cell, while Type 2 clusters contain one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 4). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. HiRel SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 5 and Figure 6 on page 7). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

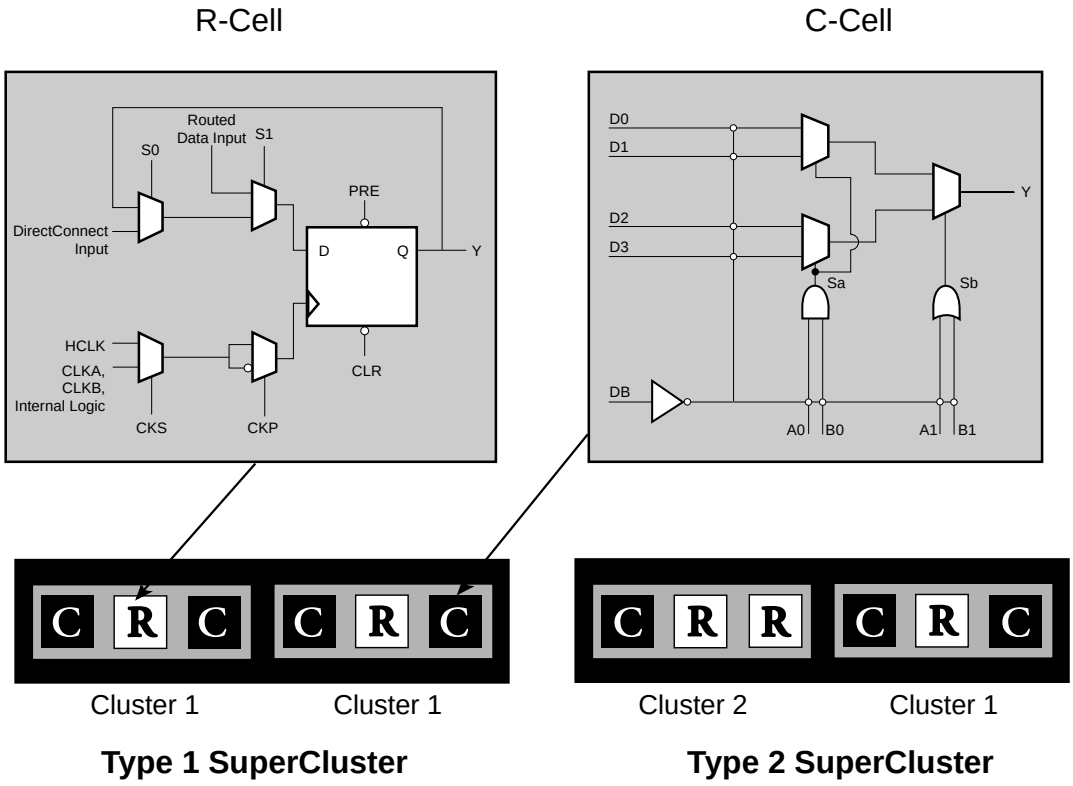


Figure 4 • *Cluster Organization*

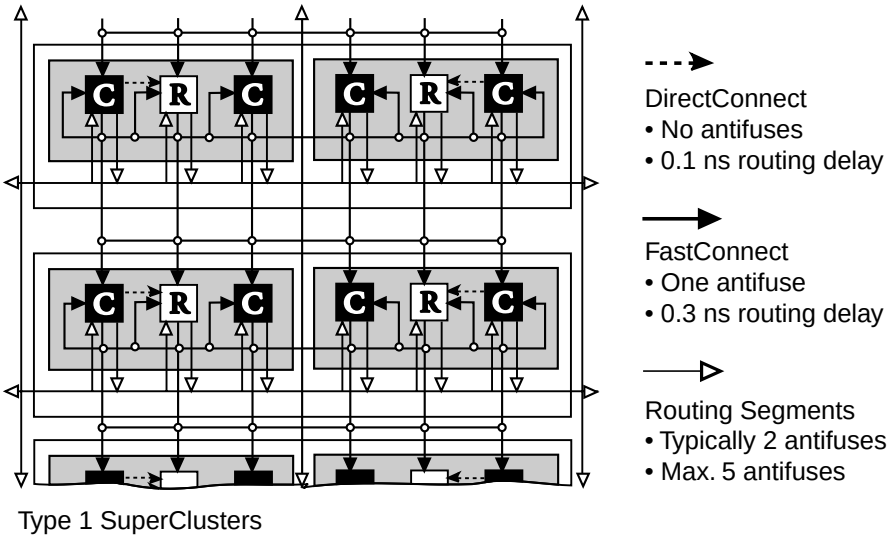


Figure 5 • *DirectConnect and FastConnect for Type 1 SuperClusters*

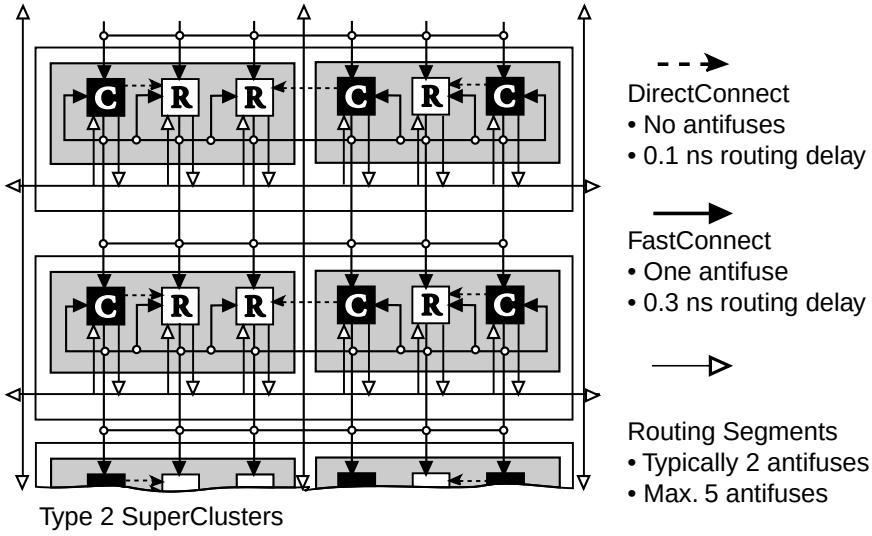


Figure 6 • *DirectConnect and FastConnect for Type 2 SuperClusters*

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

Clock Resources

Actel's high-drive routing structure provides up to three clock networks (Table 1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 5.3 ns clock-to-out (pad-to-pad) performance of the HiRel SX-A devices. The hard-wired clock is tuned to provide clock skew of less than 0.3 ns worst case. If not used, this pin must be set as LOW or HIGH on the board. It must not be left floating. Figure 7 shows the clock circuit used for the HCLK.

The two routed clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the HiRel SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, then these pins must be set as LOW or HIGH on the board. They must not be left floating (except in HiRel A54SX72A, where these clocks can be configured as regular I/Os). Figure 8 describes the CLKA and CLKB circuit used in HiRel A54SX32A.

In addition, the HiRel A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. If QCLKs are not used as quadrant clocks, they will behave as regular I/Os. The CLKA, CLKB, and QCLK circuits for HiRel A54SX72A are shown in Figure 9 on page 9. For more information, refer to the "Pin Description" section on page 30.

For more information on how to use quadrant clocks in HiRel A54SX72A, refer to Actel's *Global Clock Networks in Actel's Antifuse Devices* application note.

Table 1 • HiRel SX-A Clock Resources

	HiRel A54SX32A	HiRel A54SX72A
Routed Clocks (CLKA, CLKB)	2	2
Hardwired Clocks (HCLK)	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	4

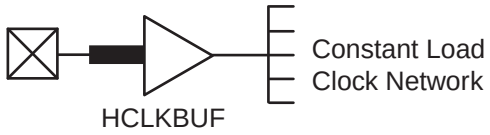
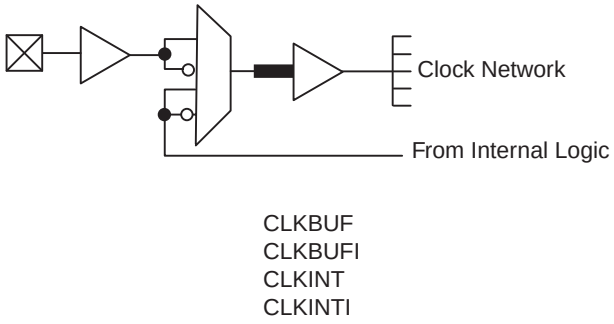


Figure 7 • HiRel SX-A Hardwired Load Clock Pad



Note: *This does not include the clock pad for HiRel A54SX72A.*

Figure 8 • HiRel SX-A Routed Clock Pads

Other Architectural Features

Technology

Actel's HiRel SX-A family is implemented in high-voltage twin-well CMOS using 0.25µm design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals. It also has a programmed ("on" state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables HiRel SX-A devices to operate with internal clock frequencies of 240 MHz, enabling very fast execution of complex logic functions. Thus, the HiRel SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet

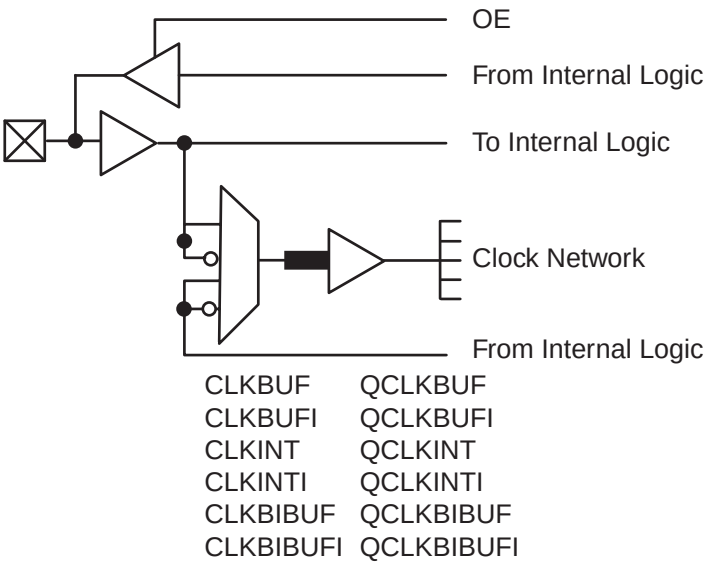


Figure 9 • *HiRel A54SX72A CLKA/CLKB/QClock Pads*

performance goals can now be integrated into a HiRel SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With HiRel SX-A devices, designers do not need to use complicated performance-enhancing design techniques, such as redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on a HiRel SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards are allowed and can be set on an individual basis. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-output-pad timing as fast as 4.1ns. In most FPGAs, I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in HiRel SX-A FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn, enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by Designer software. Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O to a known state during power up. Just slightly before V_{CCA} reaches 2.5V, the resistors are disabled, so the I/Os will behave normally. For more information about the power-up resistors, please see Actel's application note *SX-A and RT54SX-S Devices in Hot-Swap and Cold Sparing Applications*. See Table 2 and Table 3 on page 10 for more information concerning I/O features.

HiRel SX-A inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the HiRel SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below spec for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5V to provide the logic '1' input, and V_{CCI} is set to 3.3V on the HiRel SX-A device, the input signal may be pulled down by the HiRel SX-A input.

Hot Swapping

HiRel SX-A I/Os can be configured to be hot swappable in compliance with Compact PCI Specification. However, a 3.3V PCI device is not hot swappable. During power up/down, all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power up/down. After the HiRel SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Table 4 on page 10 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for a HiRel SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5V. Refer to Actel's application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications* for more information on hot swapping.

Table 2 • I/O Features

Function	Description
2 Input Buffer Threshold Selections	• 5V: PCI,TTL • 3.3V: PCI, LVTTL
Flexible Output Driver	• 5V: PCI, TTL • 3.3V: PCI, LVTTL
Output Buffer	"Hot-Swap" Capability (3.3V PCI is not hot swappable) • I/O on an unpowered device does not sink current • Can be used for "cold sparing" Selectable on an individual I/O basis Individually selectable slew rate, high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. No slew is changed on the rising edge of the output or any inputs.
Power Up	Individually selectable pull-ups and pull-downs during power up (default is to power up in tristate) Enables deterministic power up of device V_{CCA} and V_{CCI} can be powered in any order

Table 3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-up Resistor Pull
TTL, LVTTL	Yes	Yes. Affects falling edge outputs only	Pull up or Pull down
3.3V PCI	No	No. High slew rate only	Pull up or pull down
5V PCI	Yes	No. High slew rate only	Pull up or pull down

Table 4 • Power-up Time at which I/Os Become Active

Ramp Rate	0.25V/µs	0.025V/µs	5V/ms	2.5V/ms	0.5V/ms	0.25V/ms	0.1V/ms	0.025V/ms
Units	µs	µs	ms	ms	ms	ms	ms	ms
HiRel A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
HiRel A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Power Requirements

The HiRel SX-A family supports 2.5V/3.3V/5V mixed-voltage operation and is designed to tolerate 5V inputs for all standards except for 3.3V PCI. In PCI mode, I/Os support 3.3V/5V, and input tolerance depends on V_{CCI}. (Refer to the following tables for more information: "3.3V LVTTL and 5V TTL Electrical Specifications" table on page 13 and "DC Specifications (5V PCI Operation)" table on page 14). Power consumption is extremely low due to the very short distances signals required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power architecture on the market.

Boundary Scan Testing (BST)

All HiRel SX-A devices are IEEE 1149.1 compliant. HiRel SX-A devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible (Table 5). TMS cannot be employed as user I/Os in either mode.

Table 5 • Boundary Scan Pin Functionality

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10kΩ on TMS

Configuring Diagnostic Pins

The JTAG and Probe pins (TDI, TCK, TMS, TDO, PRA, and PRB) are placed in the desired mode by selecting the appropriate check boxes in the “Variation” dialog window. This dialog window is accessible through the Design Setup Wizard under the Tools menu in Actel’s Designer software.

If JTAG I/Os (except TMS) are not programmed as dedicated JTAG I/Os, they can be used as regular I/Os.

TRST Pin

When the "Reserve JTAG Test Reset" box is checked, the TRST pin will become a Boundary Scan Reset pin. In this mode, the TRST pin will function as a dedicated, asynchronous, active-low input to initialize or reset the BST circuit. An internal pull-up resistor will be automatically enabled on the TRST pin.

The TRST pin will function as a user I/O when the "Reserve JTAG Test Reset" box is not checked. The internal pull-up resistor will be disabled in this mode.

Dedicated Test Mode

When the “Reserve JTAG” box is checked in the Designer software, the HiRel SX-A device is placed in Dedicated Test mode, which configures the TDI, TCK, and TDO pins for BST or in-circuit verification with Silicon Explorer II. An internal pull-up resistor is automatically enabled on both the TMS and TDI pins. In dedicated test mode, TCK, TDI, and TDO are dedicated test pins and become unavailable for pin assignment in the Pin Editor. The TMS pin will function as specified in the IEEE 1149.1 (JTAG) Specification.

Flexible Mode

When the “Reserve JTAG” box is not selected , the HiRel SX-A device is placed in flexible mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or BST pins. In this mode the internal pull-up resistors on the TMS and TDI pins are disabled. An external 10kΩ pull-up resistor to V_{CCI} is required on the TMS pin.

The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logical low. Once the BST pins are in test mode, they will remain in BST mode until the internal BST state machine reaches the “logic reset” state. At this point the BST pins will be released and will function as regular I/O pins. The “logic reset” state is reached five TCK cycles after the TMS pin is set to logical HIGH.

Development Tool Support

HiRel SX-A devices are fully supported by Actel’s line of FPGA development tools, including Actel’s Designer software and Actel Libero Integrated Design Environment (IDE), the FPGA design tool suite. Designer Software, Actel’s suite of FPGA development tools for PCs and Workstations, includes the ACTgen Macro Builder, timing driven place-and-route, timing analysis tools, and fuse file generation. Libero IDE is a design management environment that integrates the needed design tools, streamlines the design flow, manages all design and log files, and passes necessary design data between tools. Libero IDE includes, Synplify, ViewDraw, Actel’s Designer Software, ModelSim HDL Simulator, WaveFormer Lite, and Actel’s Silicon Explorer II.

HiRel SX-A Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 10 on page 12 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification. The TRST pin is equipped with an internal pull-up resistor. To remove the boundary scan state machine from the reset state during probing, it is recommended that TRST be left floating.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuit. Actel recommends that you use a series 70 Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

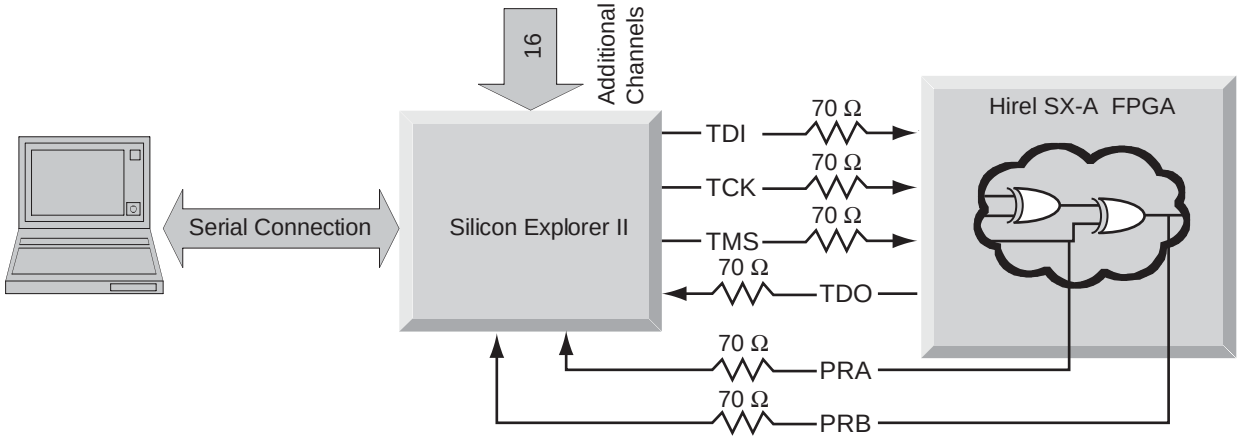


Figure 10 • *Probe Setup*

2.5V/3.3V/5V Operating Conditions

Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +6.0	V
V_O	Output Voltage	–0.5 to +V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Recommended Operating Conditions

Parameter	Military	Units
Temperature Range*	–55 to +125	°C
V_{CCA} 2.5V Power Supply Range	2.25 to 2.75	V
V_{CCI} 3.3V Power Supply Range	3.0 to 3.6	V
V_{CCI} 5V Power Supply Range	4.5 to 5.5	V

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

3.3V LVTTL and 5V TTL Electrical Specifications

Symbol	Parameter		Military Min.	Military Max.	Units
V_{OH}	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = –1mA)	0.9 V_{CCI}		V
	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = –8mA)	2.4		V
V_{OL}	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 1mA)		0.1 V_{CCI}	V
	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 12mA)		0.4	V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–20	+20	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–20	+20	µA
t_R, t_F	Input Transition Time t_R, t_F			10	ns
C_{IO}	I/O Capacitance		20	10	pF
I_{CC}	Standby Current			25	mA
IV Curve[1]	Can be derived from the IBIS model on the web.				

Notes:

1. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*
2. *See the* SX-A FPGA Family *data sheet for more information on commercial devices.*

Maximum Source and Sink Currents for all I/O Standards

I/O Standard	Max Source Current		Max Sink Current	
	Min V_{OH}	I(typ)(mA)	Max V_{OL}	I(typ)(mA)
5V TTL	2.4V	–139	0.4V	46
	0.9V_{CCI}	–35	0.1V_{CCI}	56
3.3V LVTTL	2.4V	–43	0.4V	39
	0.9V_{CCI}	–18	0.1VV_{CCI}	32
5V PCI	2.4V	–139	0.55V	61.5
3.3V PCI	0.9V_{CCI}	–20	0.1V_{CCI}	38

Note: *This information is derived from the IBIS model and was taken under typical conditions. The numbers do NOT include derating for package resistance.*

5V PCI Compliance for the HiRel SX-A Family

The HiRel SX-A family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		4.5	5.5	V
V_{IH}	Input High Voltage[1]		2.0	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pullup must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Figure 11 shows the 5V PCI V/I curve and the minimum and maximum PCI drive characteristics of the HiRel SX-A family.

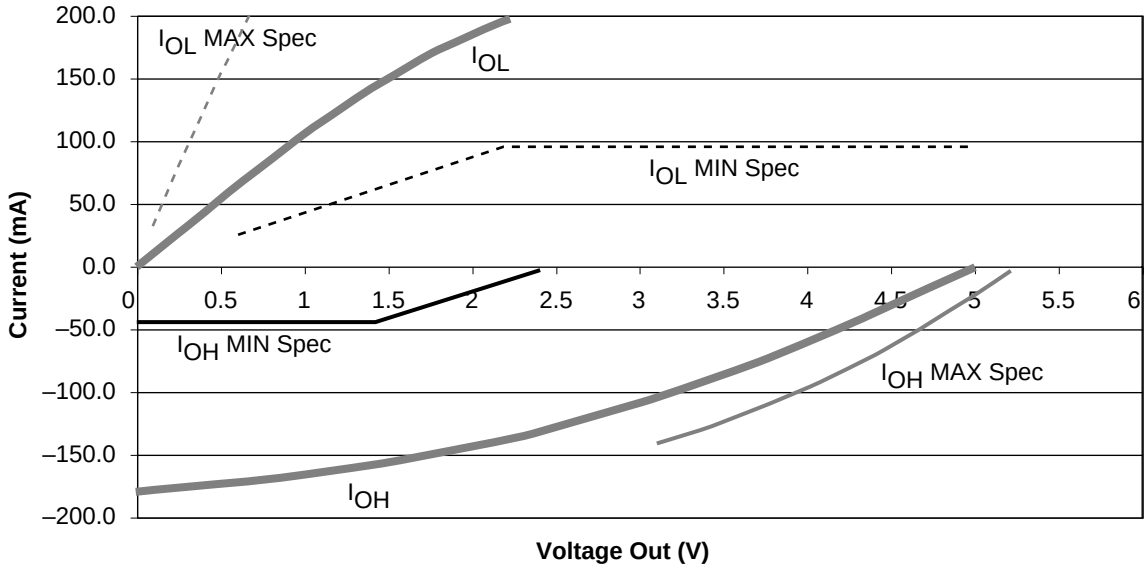


Figure 11 • *5V PCI Curve for HiRel SX-A Family*

Equation A

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$
$$\text{for } V_{CCI} > V_{OUT} > 3.1V$$

Equation B

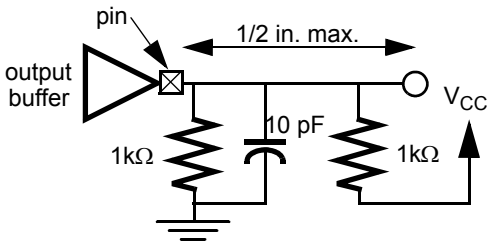
$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.71V$$

AC Specifications (5V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ [1]	–44		mA
		$1.4 \leq V_{OUT} < 2.4$ [1, 2]	$(–44 + (V_{OUT} – 1.4)/0.024)$		mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]		Equation A on page 14	
	(Test Point)	$V_{OUT} = 3.1$ [3]		–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ [1]	95		mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$		mA
		$0.71 > V_{OUT} > 0$ [1, 3]		Equation B on page 14	
	(Test Point)	$V_{OUT} = 0.71$ [3]		206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \leq –1$	$–25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V - 2.4V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V - 0.4V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 11 on page 14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 11 on page 14. The equation defined maximum should be met by the design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates. Therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise in slew rate does not apply to open drain outputs.*



3.3V PCI Compliance for the HiRel SX-A Family

The HiRel SX-A family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$		±20	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Figure 12 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the HiRel SX-A family.

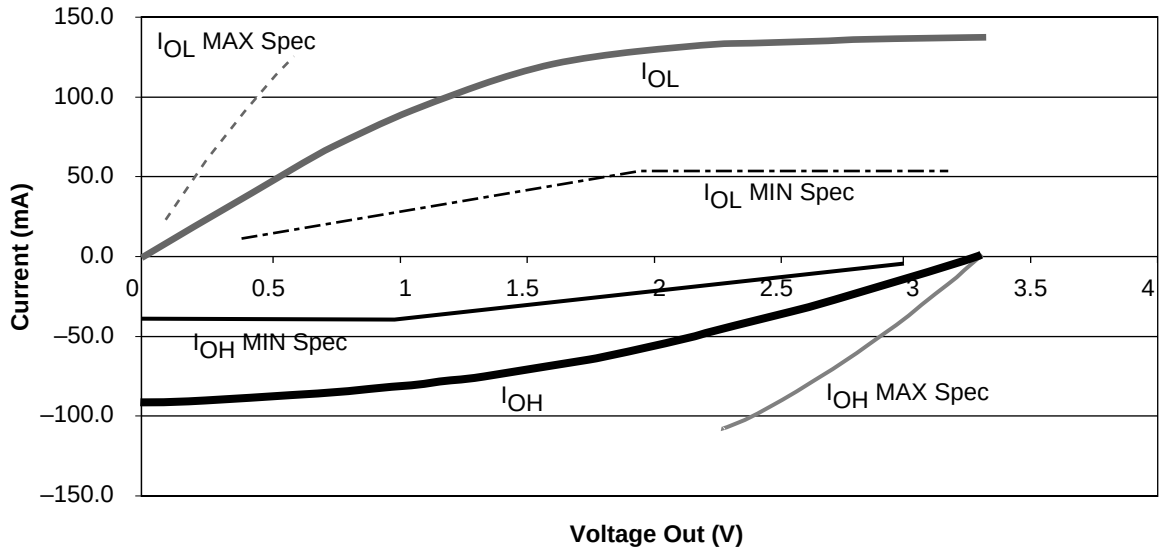


Figure 12 • *3.3V PCI Curve for HiRel SX-A Family*

Equation C

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$
$$\text{for } V_{CCI} > V_{OUT} > 0.7\ V_{CCI}$$

Equation D

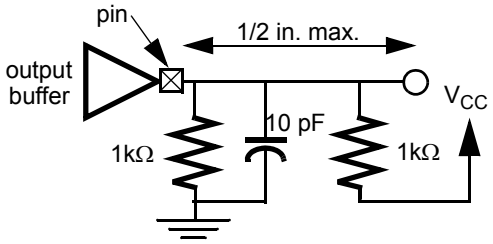
$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\ V_{CCI}$$

AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1 + (V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		Equation C on page 16	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1]	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		Equation D on page 16	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load [3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load [3]	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 12 on page 16. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 12 on page 16. The equation defined maximum should be met by the design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*



Junction Temperature (T_J)

The temperature variable that is selected in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 1, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P \quad (2)$$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics table below.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

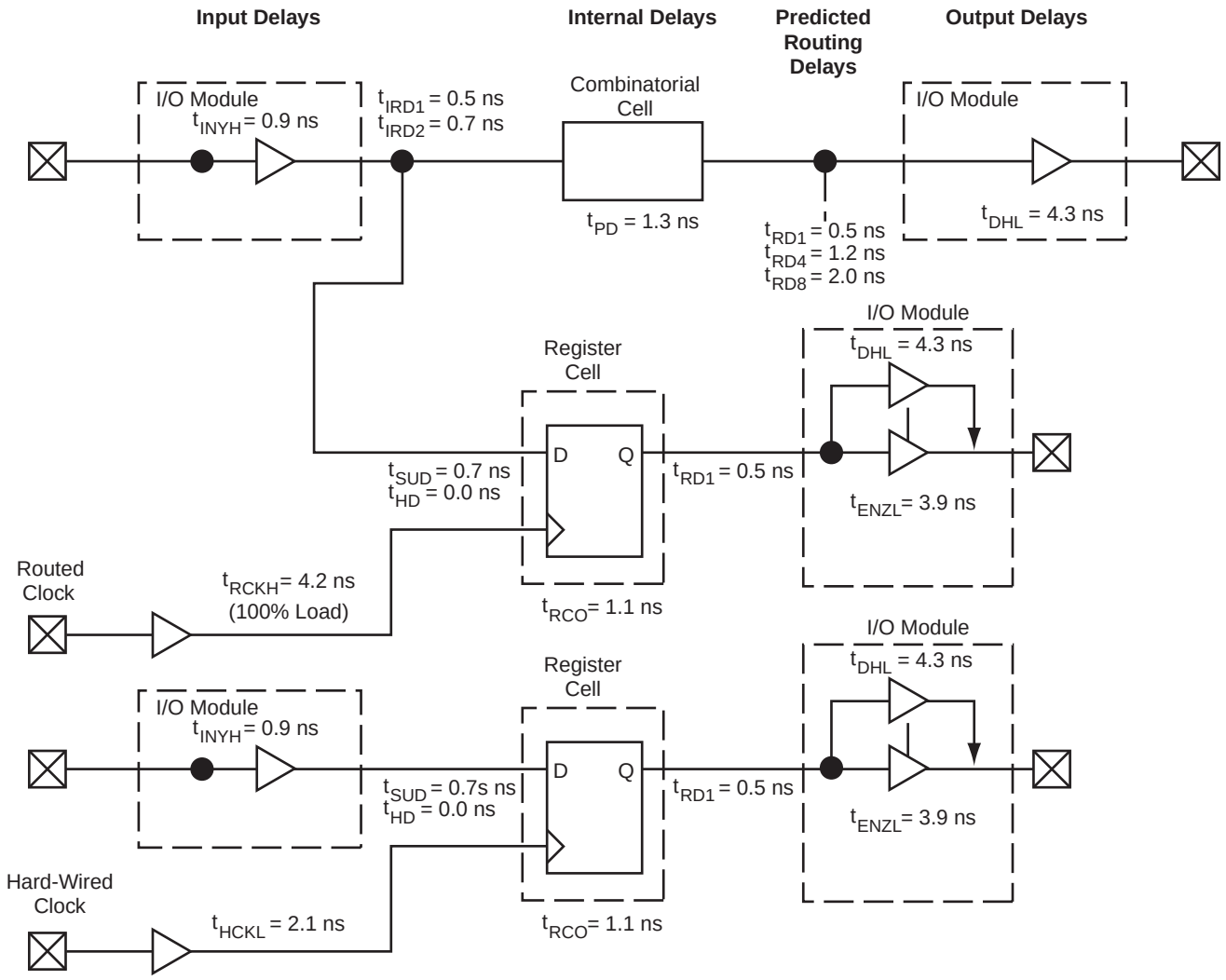
A sample calculation of the absolute maximum power dissipation allowed for a CQFP 256-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{20\text{°C/W}} = 4.0\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Ceramic Quad Flat Pack (CQFP)	208	6.3	22	14	°C/W
Ceramic Quad Flat Pack (CQFP)	256	6.2	20	10	°C/W

For Power Estimator information, please go to http://www.actel.com/products/tools/index.html.

HiRel SX-A Timing Model*



Note: **Values shown for are HiRel A54SX72A–1, worst-case military conditions for 3.3V.*

Hard-Wired Clock

External Set-Up = $t_{INYH} + t_{RD1} + t_{SUD} - t_{HCKL}$
= 0.9 + 0.5 + 0.7 – 2.1 = 0.0 ns

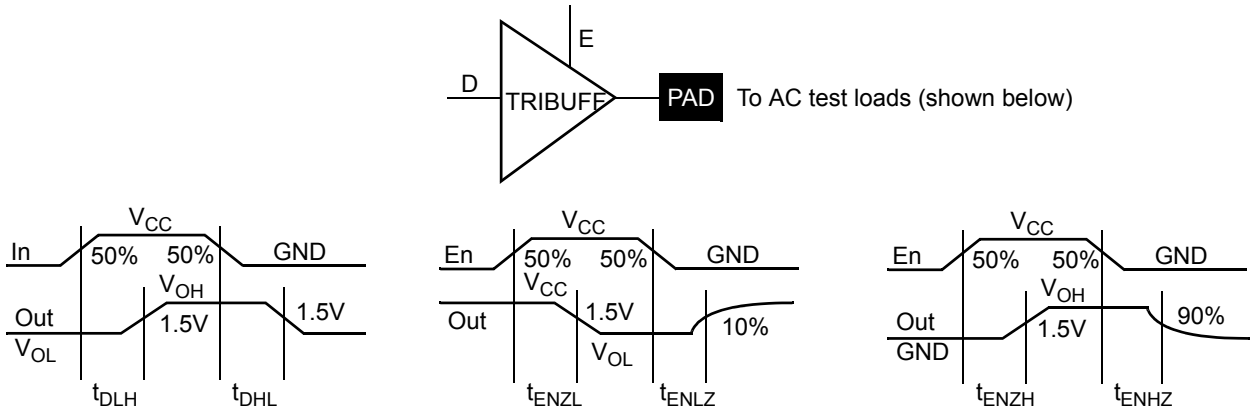
Clock-to-Out (Pin-to-Pin)
= $t_{HCKL} + t_{RCO} + t_{RD1} + t_{DHL}$
= 2.1 + 1.1 + 0.5 + 4.3 = 8.0 ns

Routed Clock

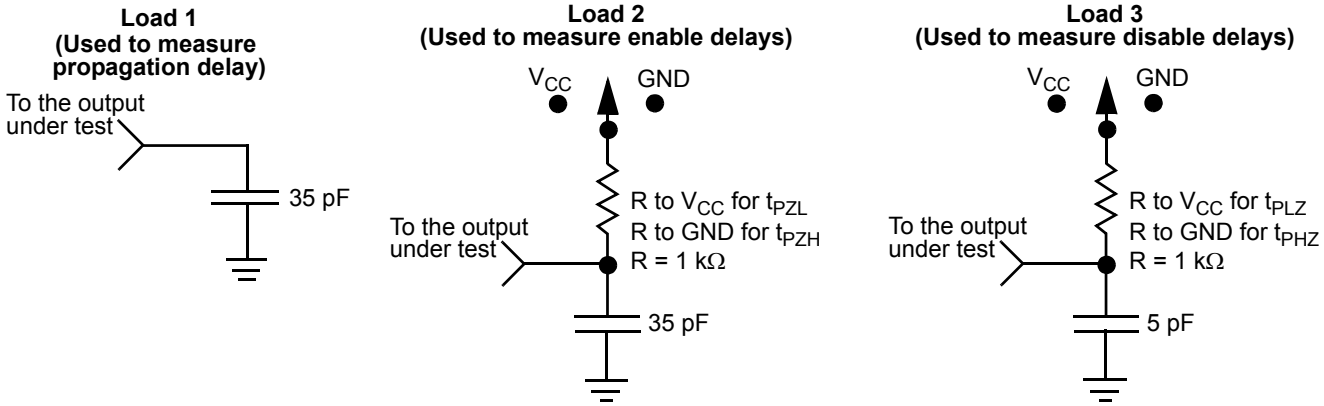
External Set-Up = $t_{INYH} + t_{RD1} + t_{SUD} - t_{RCKH}$
= 0.9 + 0.5 + 0.7 – 4.2 = -2.1 ns

Clock-to-Out (Pin-to-Pin)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 4.2+ 1.1+ 0.5 + 4.3 = 10.1 ns

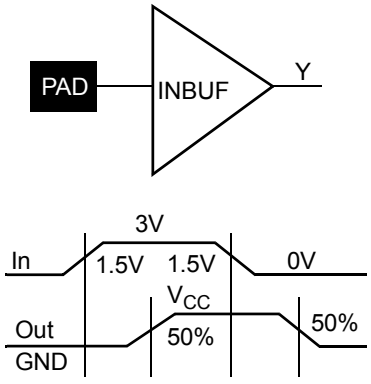
Output Buffer Delays



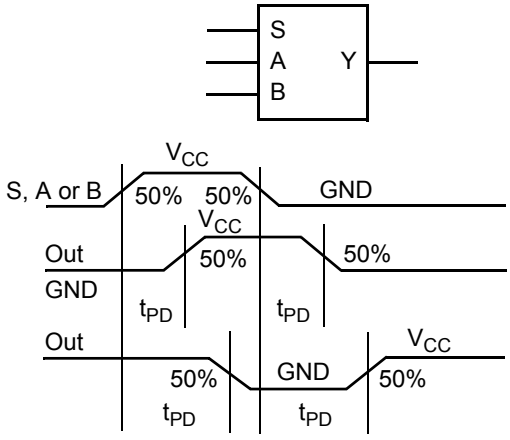
AC Test Loads



Input Buffer Delays

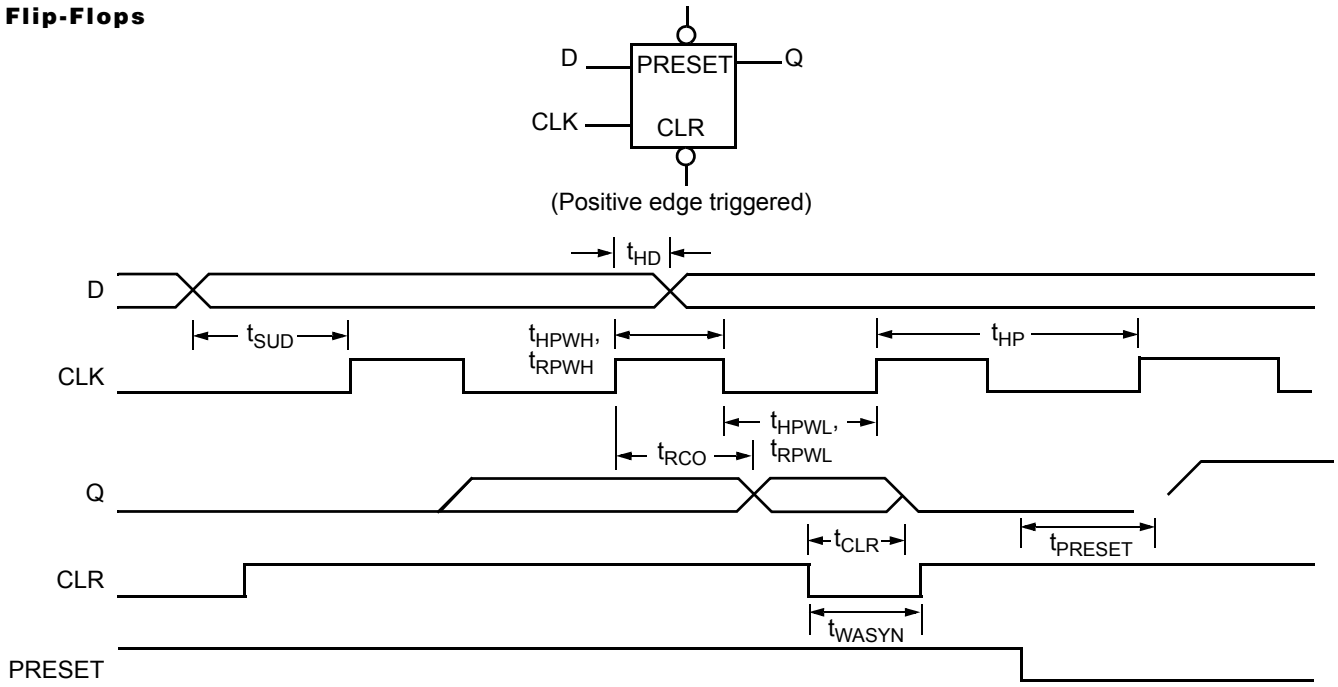


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for HiRel SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all HiRel SX-A family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the Timing Characteristics section starting on page 22.

Timing Derating

HiRel SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.3V)

V_{CCA}	Junction Temperature (T_J)						
	–55	–40	0	25	70	85	125
2.3	0.75	.079	0.88	0.89	1.00	1.04	1.16
2.5	0.70	0.74	0.82	0.83	0.93	0.97	1.08
2.7	0.66	0.69	0.79	0.79	0.88	0.92	1.02

HiRel A54SX32A Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.25V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.3		1.4	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.2		0.2	ns
t_{RD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{RD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{RD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{RD12}	FO=12 Routing Delay		2.9		3.5	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.6		1.9		ns
$t_{RECASYN}$	Asynchronous Recovery		0.4		0.5	ns
t_{HASYN}	Asynchronous Hold Time		0.4		0.5	ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		0.9		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.4		1.6	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{IRD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{IRD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{IRD12}	FO=12 Routing Delay		2.9		3.5	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

HiRel A54SX32A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.25V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.9		2.2	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.6		2.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.2		0.2	ns
t_{HP}	Minimum Period	4.2		4.9		ns
f_{HMAX}	Maximum Frequency		240		206	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.8		3.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.0		3.5	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.1		3.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.2		3.8	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.9		4.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.9		4.6	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.3		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		2.2		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.0		2.3	ns

HiRel A54SX32A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.25V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		4.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.8		4.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.4		5.1	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
3.3V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.9		5.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.3		5.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		4.9		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.2		4.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.0		5.8	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Notes:

1. *Delays based on 10pF loading.*
2. *Delays based on 35pF loading.*

HiRel A54SX32A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.25V, V_{CCI} = 4.75V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.7		5.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.2		6.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.1		6.0	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
5V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.8		4.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8		5.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.5		4.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.1		6.0	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.4		7.3	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Notes:

1. *Delays based on 50pF loading.*
2. *Delays based on 35pF loading.*

HiRel A54SX72A Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.25V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.3		1.5	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.2		0.2	ns
t_{RD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{RD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{RD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{RD12}	FO=12 Routing Delay		2.9		3.5	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.1		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.6		1.9		ns
$t_{RECASYN}$	Asynchronous Recovery		0.4		0.5	ns
t_{HASYN}	Asynchronous Hold Time		0.4		0.5	ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		0.9		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.4		1.6	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{IRD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{IRD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{IRD12}	FO=12 Routing Delay		2.9		3.5	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

HiRel A54SX72A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.25V, V_{CCI} = 3.0V, T_J = 125°C)

Dedicated (Hard-Wired) Array Clock Network		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.4		2.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.1		2.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.5		0.6	ns
t_{HP}	Minimum Period	4.2		4.9		ns
f_{HMAX}	Maximum Frequency		240		206	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.2		4.9	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		4.4		5.2	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		5.1		6.0	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		5.2		6.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		7.0		8.1	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		7.0		8.2	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.3		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.0		2.3	ns

HiRel A54SX72A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.25V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		4.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.8		4.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.4		5.1	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
3.3V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.9		5.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.3		5.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		4.9		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.2		4.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.0		5.8	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Notes:

1. *Delays based on 10pF loading.*
2. *Delays based on 35pF loading.*

HiRel A54SX72A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.25V, V_{CCI} = 4.75V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0 V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.3		5.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.2		6.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.1		5.9	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
5V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.8		4.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8		5.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.5		4.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.1		6.0	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.4		7.3	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Notes:

1. *Delays based on 50pF loading.*
2. *Delays based on 35pF loading.*

Pin Description

CLKA/B Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For HiRel A54SX72A, these clocks can be configured as user I/O.)

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only for HiRel A54SX72A. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used as a clock, it will behave as a regular I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O*, PRB, I/O* Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O* Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 5 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O* Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 5 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O* Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 5 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to a user I/O when "checksum" is complete.

TMS* Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 5 on page 10). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Test Reset Pin" is not selected in Actel's Designer software.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See the "Recommended Operating Conditions" table on page 12. All V_{CCI} power pins in the device should be connected.

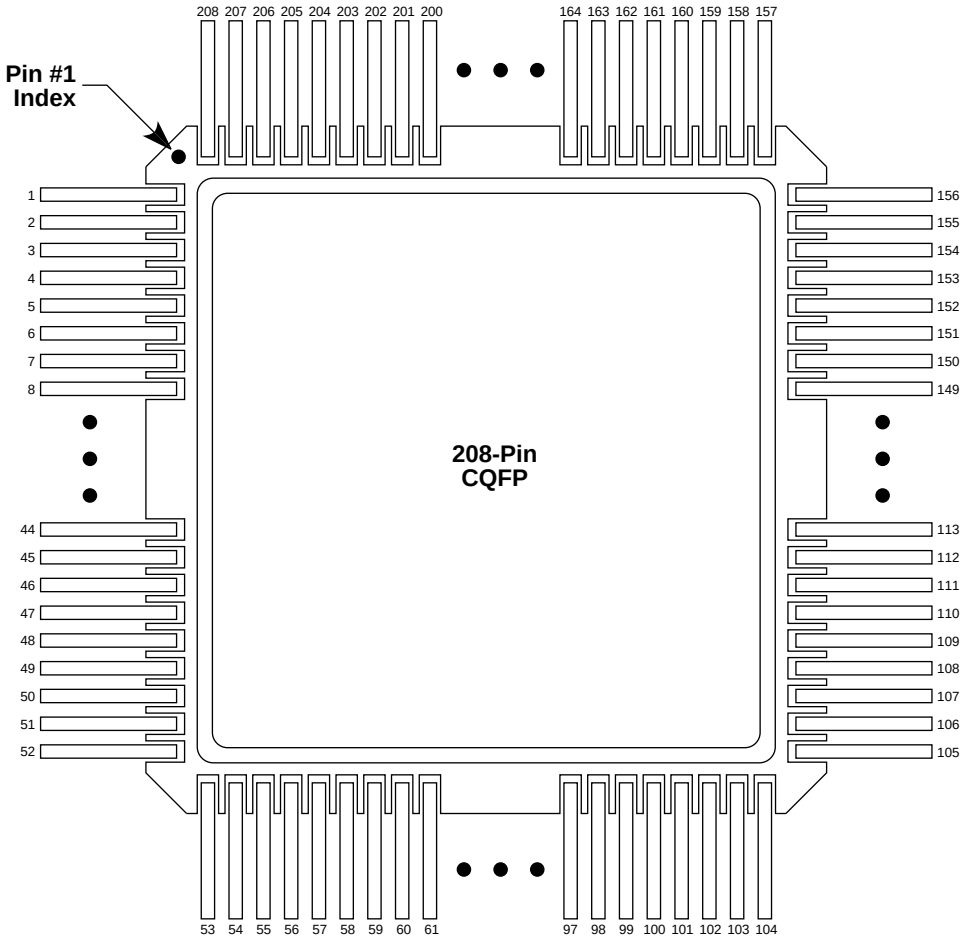
V_{CCA} Supply Voltage

Supply voltage for Array. See the "Recommended Operating Conditions" table on page 12. All V_{CCA} power pins in the device should be connected.

** 70 Ω series termination should be placed on the board to enable probing capability.*

Package Pin Assignments

208-Pin CQFP (Top View)



208-Pin CQFP

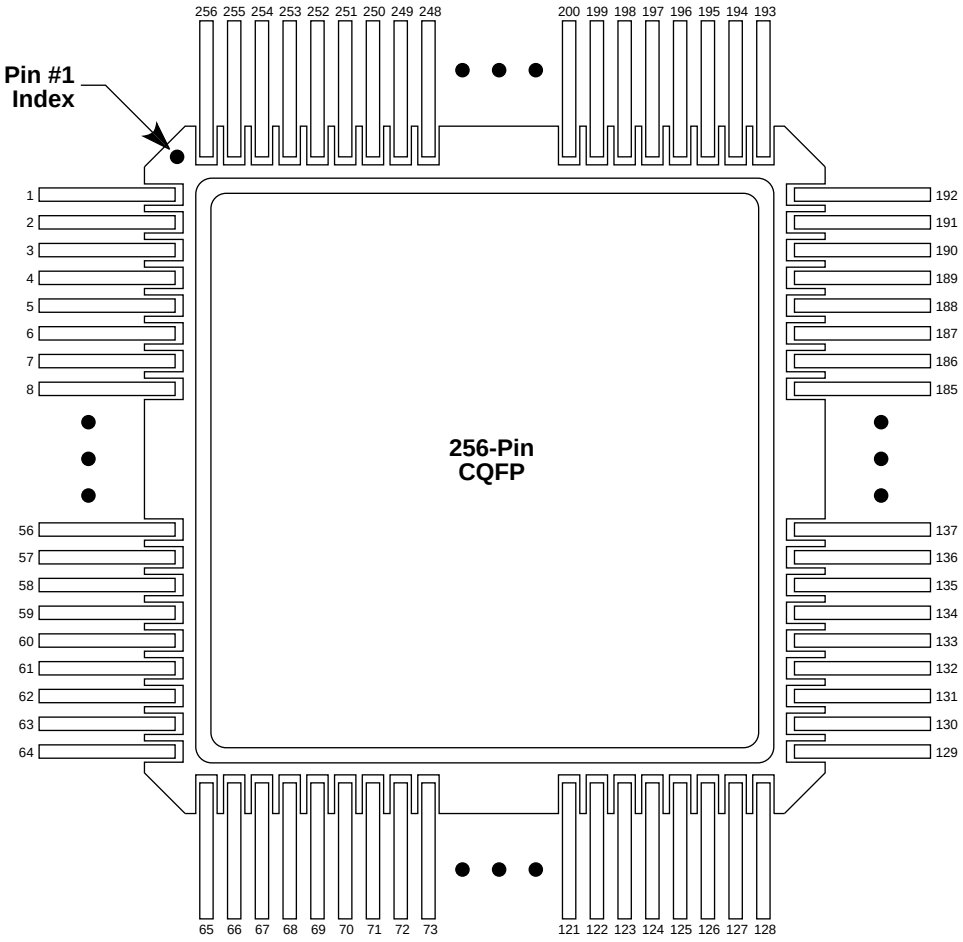
Pin Number	HiRel A54SX32A Function	HiRel A54SX72A Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	V_{CCI}	V_{CCI}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	GND
19	I/O	V_{CCA}
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	NC	I/O
26	GND	GND
27	V_{CCA}	V_{CCA}
28	GND	GND
29	I/O	I/O
30	TRST, I/O	TRST, I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	GND	GND
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	V_{CCI}	V_{CCI}
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	NC	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	QCLKA
75	I/O	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	V_{CCA}	V_{CCA}
79	GND	GND
80	NC	NC
81	I/O	I/O
82	HCLK	HCLK
83	I/O	V_{CCI}
84	I/O	QCLKB
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	I/O
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	V_{CCI}	V_{CCI}
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	TDO, I/O	TDO, I/O
104	I/O	I/O

208-Pin CQFP (Continued)

Pin Number	HiRel A54SX32A Function	HiRel A54SX72A Function
105	GND	GND
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	I/O	I/O
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}
116	I/O	GND
117	I/O	V_{CCA}
118	I/O	I/O
119	I/O	I/O
120	I/O	I/O
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	GND	GND
130	V_{CCA}	V_{CCA}
131	GND	GND
132	NC	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	I/O	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	V_{CCA}	V_{CCA}
146	GND	GND
147	I/O	I/O
148	V_{CCI}	V_{CCI}
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O
157	GND	GND
158	I/O	I/O
159	I/O	I/O
160	I/O	I/O
161	I/O	I/O
162	I/O	I/O
163	I/O	I/O
164	V_{CCI}	V_{CCI}
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	I/O	I/O
175	I/O	I/O
176	I/O	I/O
177	I/O	I/O
178	I/O	QCLKD
179	I/O	I/O
180	CLKA	CLKA
181	CLKB	CLKB
182	NC	NC
183	GND	GND
184	V_{CCA}	V_{CCA}
185	GND	GND
186	PRA, I/O	PRA, I/O
187	I/O	V_{CCI}
188	I/O	I/O
189	I/O	I/O
190	I/O	QCLKC
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	V_{CCI}	V_{CCI}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



256-Pin CQFP

Pin Number	HiRel A54SX32A Function	HiRel A54SX72A Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	V_{CCI}
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	V_{CCI}	V_{CCI}
29	GND	GND
30	V_{CCA}	V_{CCA}
31	GND	GND
32	I/O	I/O
33	I/O	I/O
34	TRST, I/O	TRST, I/O
35	I/O	I/O
36	I/O	V_{CCA}
37	I/O	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	V_{CCA}	V_{CCA}
47	I/O	V_{CCI}
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	I/O	I/O

Pin Number	HiRel A54SX32A Function	HiRel A54SX72A Function
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	GND
57	I/O	I/O
58	I/O	I/O
59	GND	GND
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	V_{CCI}
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	QCLKA
90	PRB, I/O	PRB, I/O
91	GND	GND
92	V_{CCI}	V_{CCI}
93	GND	GND
94	V_{CCA}	V_{CCA}
95	I/O	I/O
96	HCLK	HCLK
97	I/O	I/O
98	I/O	QCLKB
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	I/O	I/O
104	I/O	I/O

256-Pin CQFP (Continued)

Pin Number	HiRel A54SX32A Function	HiRel A54SX72A Function
105	I/O	I/O
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	GND	GND
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	I/O	I/O
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	I/O	I/O
119	I/O	I/O
120	I/O	V_{CCI}
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	TDO, I/O	TDO, I/O
127	I/O	I/O
128	GND	GND
129	I/O	I/O
130	I/O	I/O
131	I/O	I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	V_{CCA}	V_{CCA}
142	I/O	V_{CCI}
143	I/O	GND
144	I/O	V_{CCA}
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O
157	I/O	I/O
158	GND	GND
159	NC	NC
160	GND	GND
161	V_{CCI}	V_{CCI}
162	I/O	V_{CCA}
163	I/O	I/O
164	I/O	I/O
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CCA}	V_{CCA}
175	GND	GND
176	GND	GND
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	I/O
181	I/O	I/O
182	I/O	I/O
183	I/O	V_{CCI}
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	I/O	I/O
189	GND	GND
190	I/O	I/O
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	I/O	I/O
202	I/O	V_{CCI}
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	I/O	I/O

256-Pin CQFP (Continued)

Pin Number	HiRel A54SX32A Function	HiRel A54SX72A Function
209	I/O	I/O
210	I/O	I/O
211	I/O	I/O
212	I/O	I/O
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O
216	I/O	I/O
217	I/O	I/O
218	I/O	QCLKD
219	CLKA	CLKA
220	CLKB	CLKB
221	V_{CCI}	V_{CCI}
222	GND	GND
223	NC	NC
224	GND	GND
225	PRA, I/O	PRA, I/O
226	I/O	I/O
227	I/O	I/O
228	I/O	V_{CCA}
229	I/O	I/O
230	I/O	I/O
231	I/O	QCLKC
232	I/O	I/O
233	I/O	I/O
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	GND
241	I/O	I/O
242	I/O	I/O
243	I/O	I/O
244	I/O	I/O
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	I/O
249	I/O	V_{CCI}
250	I/O	I/O
251	I/O	I/O
252	I/O	I/O
253	I/O	I/O
254	I/O	I/O
255	I/O	I/O
256	TCK, I/O	TCK, I/O

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (Advanced v1.2)	Page
Advanced v1.1	The "3.3V LVTTL and 5V TTL Electrical Specifications" table on page 13 was updated.	page 13
	The "DC Specifications (3.3V PCI Operation)" table on page 16 was updated.	page 16
Preliminary v1.0	The "Ordering Information" section on page 2 was updated.	page 2
	Figure 1 on page 4 was updated.	page 4
	The "Clock Resources" section on page 8 was updated.	page 8
	The "I/O Modules" section on page 9 and Table 2 on page 10 were updated.	page 9
	The "Hot Swapping" section on page 9 was updated.	page 9
	Table 3 and Table 4 on page 10 are new.	page 10
	The "Power Requirements" section on page 10 was updated.	page 10
	The "Design Considerations" section on page 11 was updated.	page 11
	Figure 10 on page 12 was updated.	page 12
	The "Absolute Maximum Ratings*" table on page 12 and the "Recommended Operating Conditions" table on page 12 were updated.	page 12
	The "Maximum Source and Sink Currents for all I/O Standards" table on page 13 is new.	page 13
	The "HiRel SX-A Timing Model*" figure on page 19 was updated.	page 19
	The "Pin Description" section on page 30 was updated.	page 30
Advanced v0.1	"Clock Resources" section on page 8 has been updated.	8
	"I/O Modules" section on page 10 has been updated.	9
	"Hot Swapping" section on page 9 has been updated.	9
	"Power Requirements" section on page 10 has been updated.	9
	"Boundary Scan Testing (BST)" section on page 11 has been updated.	10
	"Configuring Diagnostic Pins" section on page 11 has been updated.	10
	"TRST Pin" section on page 11 has been updated.	10
	"Dedicated Test Mode" section on page 11 has been updated.	10
	"Development Tool Support" section on page 11 has been updated.	10
	"HiRel SX-A Probe Circuit Control Pins" section on page 11 has been updated.	10
	"Pin Description" section on page 30 has been updated.	32
	Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as “Product Brief,” “Advanced,” “Production,” and “Web-only.” The definition of these categories are as follows:

Product Brief

The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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