Analysis of SDI/DCLK Issue for RH1020 and RT1020

Background

The SDI and DCLK pins (pin numbers 61 and 62, respectively) do not function properly when configured as outputs on all Actel RT1020 devices and older RH1020 devices. This problem does not exist on RH1020 devices manufactured in mid-1999 or later and designated as "pass 8" silicon. In normal mode, the user must program the security fuse ("program fuse") in order to configure SDI and DCLK pins as outputs. However, as a result of the issue described in this report, the SDI/DCLK output configuration is not supported in the affected devices. This technical brief discusses the cause of this phenomenon, and its impact on reliability.

Functional Description

When SDI and DCLK are configured as outputs, the "program fuse" must be blown, as discussed in the *RadHard/RadTolerant Programming Guide* in table 1-2 on page 22, located on Actel's web site. When the "program fuse" is programmed, node 1 (as shown in Figure 1) becomes a logic "0." Node "SFUSBLO," which is the output-enable for SDI and DCLK pins should become a logical "1" (5 volts). In the design, there exists a latch that consists of inverters 2 and 3. The latch's function is to pull and keep node "SFUSBLO" at V_{CC} (logical "1").

Failure Description

SDI and DCLK become tristated when configured as outputs and the supply voltage is below 5.0 volts. However, if the voltage is increased to 6.0 volts and then decreased to 3.5 volts, the two outputs function properly.

Analysis

An experiment was performed to determine the state of the special I/Os: SDI and DCLK. A simple design was generated to use the SDI and DCLK pins as outputs ("program fuse" was blown). In addition, a 10K Ohm resistor was placed in series with the output pins (SDI/DCLK) to limit current flow. The output of SDI and DCLK could be pulled up in the experiment (resistor connected to V_{CC}), a characteristic of a tristated output.

Failure Mechanism

Figure 1 shows a simplified schematic diagram of the silicon signature portion of the circuit. Note: SFUSBLO is the point of interest since it must be a logic "1" to enable the output buffers of SDI and DCLK. This condition occurs when the "program fuse is blown."

Initially, the anomalous behavior was attributed to the high fuse resistance (due to the non-ideal programming path). However, an experiment proved this assumption inaccurate. Node 1 was shorted to GND, thus bypassing the fuse, using Focus Ion Beam (FIB) technology. With node 1 at logic "0," the output of SDI and DCLK remained tristated. This was further supported by SPICE simulation. (See "Appendix A" on page 4)

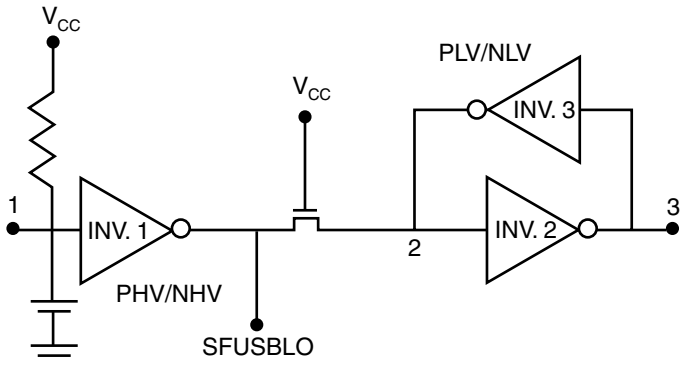


Figure 1 • *Simplified Silicon Signature Circuit*

Initially, when the "program fuse" is not blown, (unblown program fuse symbolized as a capacitor in Figure 1 on page 1, from node 1 to ground) node 1 is a logic "1." Nodes SFUSBLO and 2 (because the pass device is turned on) will be at logic "0" (0 volts).

For the purpose of this discussion, assume that nodes SFUSBLO and 2 are the same, since the pass device is on. When the "program fuse" is blown, node 1 has a path to ground, by way of a ruptured program fuse, and becomes a logic "0." Node SFUSBLO will begin making a transition from L->H (logic "0" to "1"). Simultaneously, since node 3 is initially "1," the NLV (NMOS, low voltage device in inverter 3) device is fully turned on, thereby causing the output of inverter 3 (SFUSBLO) to be "0." Since the output of inverter 3 is a logical "0" (0 volts) and the output of inverter 1 is a logical "1" (5 volts) (due to the programmed antifuse), we now have a state of contention. Bench microprobing of the SFUSBLO signal at Actel indicates that node SFUSBLO is at ~2.0V when the SDI/DCLK pins are not functioning as outputs. Please refer to Figure 2 for a simplified drawing of this effect. The p-channel of inverter 1 is constructed with a thick oxide of 350 angstroms.

This is a high voltage p-channel (PHV) device. The n-channel device in inverter 3 is a standard low voltage (oxide thickness of 190 angstroms) n-channel device, referred to as NLV. The final state is determined by the strongest device (NLV in this circuit, since PHV is especially weak in the RH process), which will cause SFUSBLO to stay at logic "0." Hence, it is crucial that the ratio of the ldsat(NLV)/ldsat(PHV) is correct. From previous simulations, the optimum ldsat(NLV)/ldsat(PHV) was found to be 4.7 for a commercial 1020 device. However, due to the difference in processes between commercial and RadHard devices, the ldsat(NLV)/ldsat(PHV) ratio is 7.9 (for the RH process).

Effects On Reliability

Figure 3 shows the resultant circuit when the aforementioned phenomenon occurs. The current passes through a high-voltage PMOS pull-up, an NMOS pass transistor, and a NMOS pull down to ground. Although the potential increase in current is likely, it is not significant enough to be measured on the bench. SPICE simulations (refer to "Appendix B" on page 5) show that the worst case increase in ldd is 240µA (at +25°C) and 350µA (-55°C). However, analyses performed by Actel (including radiation effects) indicate that this current is too low to cause any reliability issue, such as dielectric rupture, hot carrier degradation, or electromigration. Explanations are as follows:

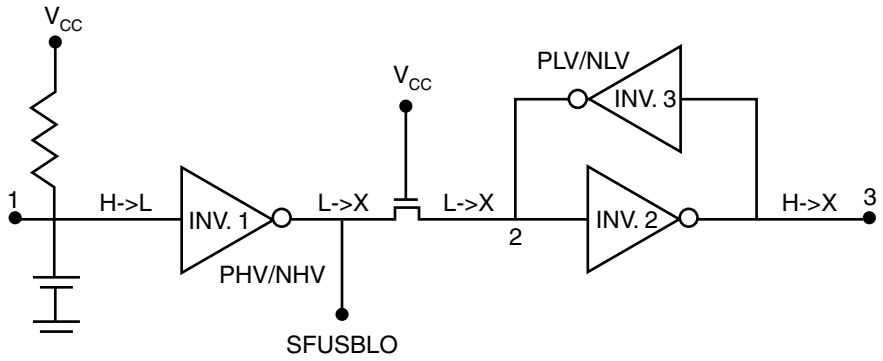


Figure 2 • *State of nodes 1, 2, and 3 when "program fuse" is programmed*

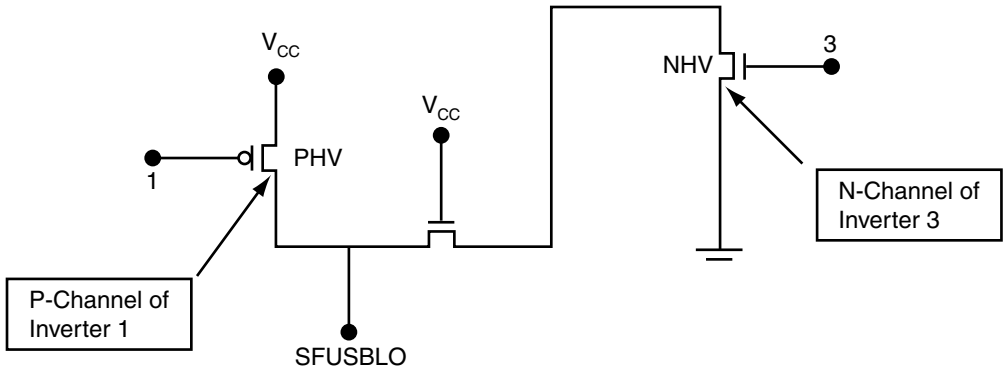


Figure 3 • *Schematic Diagram of the Effects of Both NLV and PHV on*

Hot Carrier (Figure 4)

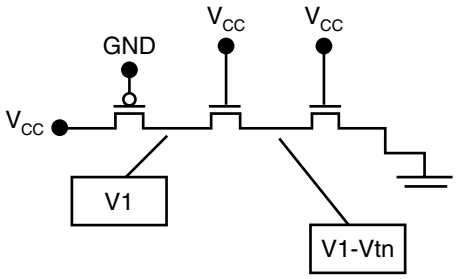


Figure 4 • *Hot Carrier Effect*

It is well known that as NMOS channel lengths are reduced, the electric field at the drain of a transistor in saturation increases (for a fixed drain voltage). The electric field can become so high that electrons acquire enough kinetic energy to become what is termed "hot." These hot electrons can penetrate the gate oxide layer and produce a gate current. The trapping of charges injected into the oxide can, eventually, lead to degradation of the MOS device parameters such as threshold, subthreshold current, and transconductance, which in turn could lead to failures in circuits. For p-channel devices, since the mobility of holes is much less than that of the electrons in the n-channel device, there is no risk of hot holes. Thus the hot electron effect is limited to the n-channel devices and is a strong function of both the Vds voltage and the channel length of the device.

In the case of the circuit shown above, both n-channel devices are larger than minimum channel length (by 2.2µm) and exhibit a lower Vds voltage than the worst case characterized at 5.5V. For transistor (1), the effective Vds is equivalent to the threshold drop of the transistor. For transistor (2), the effective Vds, when the circuit is non-functional, is equivalent to V1-Vtn, where V1 was measured to be ~2.0V. In summary, there is no hot carrier issue with this circuitry.

Electromigration

Electromigration refers to the displacement of atoms within the conducting material (metals). This displacement is due to the transfer of momentum from the mobile carriers to the atomic lattices and vice versa. When a high current passes through thin metal conductors in integrated circuits, metal ions in some regions will pile up and voids will form in other regions. Thus, discontinuity in metal conductors can occur.

In the case of the circuit shown above, the maximum current through simulation was found to be 240µA at +25°C and 350µA at -55°C. Based on the layout dimensions, the maximum current density, J (mA/µm), through this circuit is:

J = Idd (worst case)/ W_{min}; where W_{min} = 2.7µm

was calculated to be 0.09mA/µm (+25°C) and 0.13mA/µm (-55°C), where the process was designed for a minimum current density of 1.0mA/µm. For room temp, there is 10X margin to electromigration. It is known that electromigration is a function of temperature as illustrated in the following equation:

MTF ~ l/J2->1/J^2

thus there is additional margin at -55°C due to the temperature effects. At hot temp, the Idd current is significantly reduced as both the n-channel and the p-channel devices become weaker.

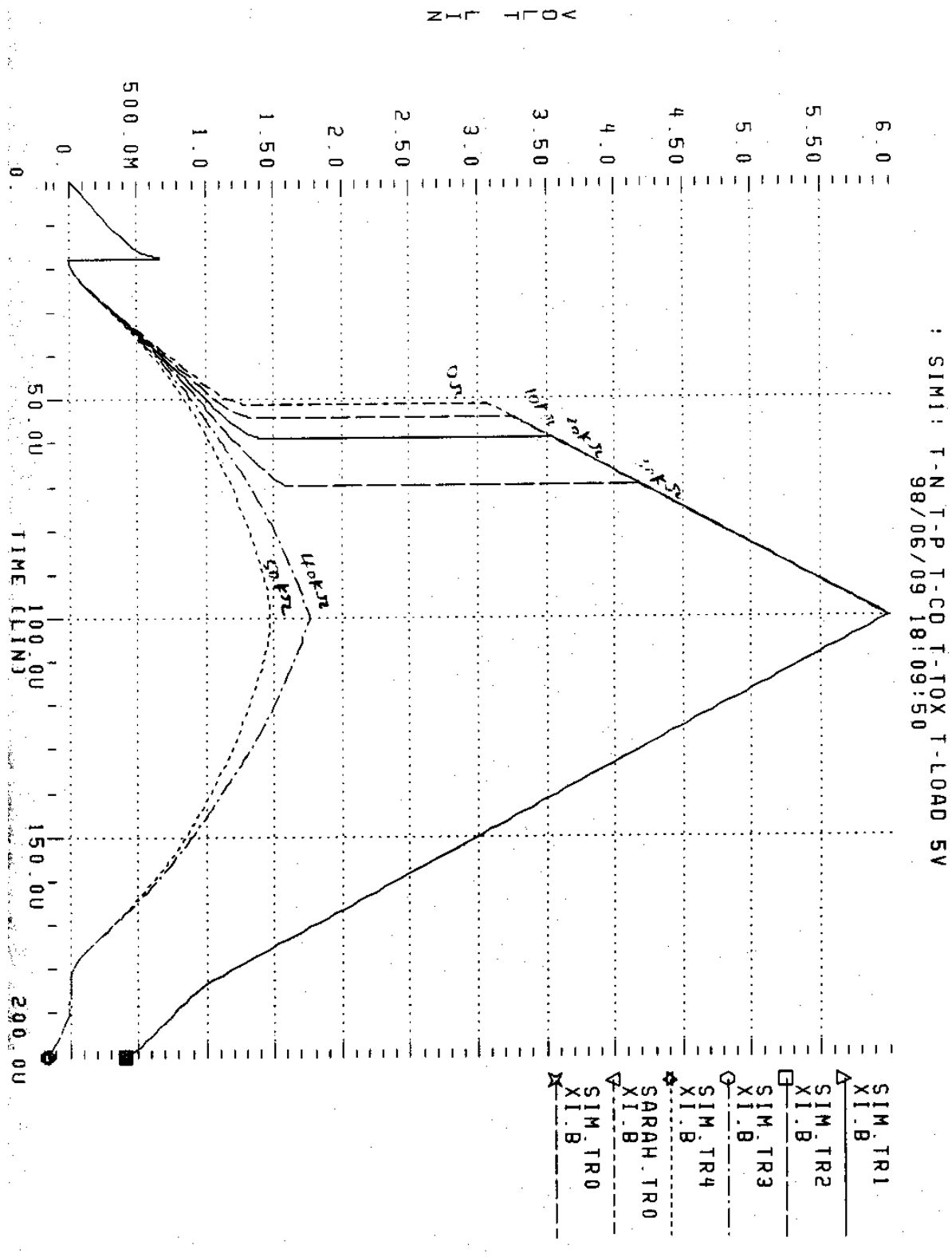
Conclusion

The security feature of blowing the program fuse is functional for all RT1020 and RH1020 devices. There is no impact on the performance or reliability of these devices by programming the security fuse (program fuse). The feature of the SDI/DCLK pins functioning as outputs is not supported in the RT1020 or early ("pass 7") RH1020 devices.

Corrective Action

Actel has implemented a fix for RH1020 devices to allow designers to use the SDI/DLK pins as outputs designated as "pass 8" material. No silicon fix is planned for RT1020 devices. We have also reviewed the circuitry to ensure that no other similar failures exist due to the weakness of the PHV devices.

Appendix A


VOLTIN
6.0
5.50
5.0
4.50
4.0
3.50
3.0
2.50
2.0
1.50
1.0
500.0M
0
0.
50.0U
100.0U
150.0U
200.0U
TIME (LIN)
: SIM1: T-N T-P T-CO T-TOX T-LOAD 5V
98/06/09 18:09:50
SIM.TR1
XI.B
SIM.TR2
XI.B
SIM.TR3
XI.B
SIM.TR4
XI.B
SARAH.TR0
XI.B
SIM.TR0
XI.B

Appendix B

lmfs0.8um

```
      jsw=     2.27p amp          php=  943.44m volt        cjp=  172.12p farad
       bv=    20.00  volt          ct     0.     secs         m   500.00m
       eg=     1.11  ev            rs=    0.     ohms

  *** name:      0:ideal              comp=  -55.0000

       is=  1.0e-28 amp            pb=  921.49m volt        cjo=     0.     farad
      jsw=     0.    amp          php=  921.49m volt        cjp=     0.     farad
       bv=     0.    volt          tt     0.     secs         m=   500.00m
       eg=     1.11  ev            rs=    0.     ohms


*** mosfet element parameters
name             rd eff   rs eff   cdsat    cssat     vto      beta


   0:m1         797.35   797.36  2.3e-17  2.3e-17    1.12    104.39u
   0:m2           2.07     2.07  4.4e-22  4.4e-22  822.23m    7.74m
   0:m3           4.07     4.07  4.4e-22  4.4e-22  752.69m   92.46u
******  Star-HSPICE  --    97.1   (970317) 13:49:58  98/08/06    solaris

******
: test: t-n t-p t-cd t-tox t-load 5v

 ******  operating point information      tnom=  25.000 temp= -55.000

******
***** operating point status is all       simulation time is     0.
   node    -voltage       node    -voltage       node    =voltage


+0:in      =   1.5942  0:vcc      =   5.0000  0:vl       =   1.4045



maximum nodal capacitance=   7.271E-14         on node     0:vcc

   nodal  capacitance table

   node          cap        node     =    cap        node     =    cap


+0:in      -  24.4487f 0:vcc      =  72.7081f 0:vl       =  29.0552l



****  voltage sources


subckt
element  0:vcc
 volts       5.0000
 current  -358.9272u
 power       1.7946m


         total voltage source power dissipation=    1.7946m       watts


**** mosfets


subckt
element   0:m1        0:m2        0:m3
model     0:phv.2     0:nmos.1    0:nmos.2
 id        358.9272u   358.9272u   358.9272u
 ibs       7.221e-17  -6.148e-22  -6.395e-25
 ibd       6.625e-18  -6.971e-22  -6.138e-22
 vgs        -1.5942      3.5955      5.0000
 vds         3.4058    189.7087m     1.4045
 vbs         3.4058     -1.4045      0.
 vth        -1.1886      1.0446    752.9261m
 vdsat      -2.7661      1.5255      3.5188
 beta       68.5738u   255.7624u    76.3507u
 gam eff   956.9586m   288.3081m   266.5996m
 gm        167.4208u   113.3366u    86.8116u
 gds         1.9133u     1.6798m   196.7576u
 gmb        45.3953u    12.8234u    14.5128u
 cdtot      18.1620f    13.4709f    14.9611f
 cgtot      11.2118f    14.4259f    20.4447f
 cstot      10.9779f    14.0941f    19.0449f
 cbtot      19.6755f     8.6360f     9.1750f
 cgs         2.7439f     7.1815f    10.9788f
 cgd         7.5942f     6.8447f     8.1323f



          ***** job concluded
******  Star-HSPICE  --    97.1   (970317) 13:49:58  98/08/06    solaris
******
: test: t-n t-p t cd t tox t load 5v
 ******  job statistics summary           tnom=  25.000 temp= -55.000
******

          total memory used        450 kbytes

 # nodes -      10 # elements-      4
 # diodes=       0 # bjts     =     0 # jfets    =     0 # mosfets =     3

   analysis      time      # points   tot. iter  conv.iter

   op point        0.03          1         14
   readin          0.62
   errchk          0.12
   setup           0.01
   output          0.00
          total cpu time          0.78 seconds
              job started at   13:49:58  98/08/06
              job ended   at   13:50:01  98/08/06
```

test.out

```
     jsw=    3.51u amp        php=   574.93m volt       cjp=   174.18p farad
      bv=   20.00  volt        tt=     0.    secs         m=   500.00m
      eg=    1.11  ev          rs=     0.    ohms

  *** name:      0:ideal              temp    125.000

      is=  5.5e-19 amp         ph=   634.86m volt       cjo=     0.    farad
     jsw=     0.    amp        php=   634.86m volt       cjp=     0.    farad
      bv=     0.    volt        tt=     0.    secs         m=   500.00m
      eg=    1.11  ev          rs=     0.    ohms


*** mosfet element parameters
name            rd eff   rs eff   cdsat     cssat      vto       beta

   0:m1         797.36   797.36    97.94p    97.94p     1.51     47.75u
   0:m2           2.07     2.07     1.29n     1.29n   822.23m     3.14m
   0:m3           4.07     4.07     1.29n     1.29n   752.69m    37.50u
******  Star HSPICE  --     97.1   (970317) 15:10:36  98/08/14    solaris

******
: test: t-n t-p t-cd t-tox t-load 5v

 ******  operating point information       tnom=  25.000 temp= 125.000

******
***** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node     voltage

+0:in          1.8033  0:vcc     =   5.0000  0:vl      =   1.5873


maximum nodal capacitance=   7.5668-14          on node     0:vcc

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:in      =  23.9705f 0:vcc     =  75.6578f 0:vl      =  28.6763f


****  voltage sources


subckt
element  0:vcc
 volts      5.0000
 current -162.6068u
 power    813.0340u

                total voltage source power dissipation=  813.0340u       watts

**** mosfets

subckt
element  0:m1       0:m2       0:m3
model    0:phv.2    0:nmos.1   0:nmos.2
 id       162.6065u  162.6045u  162.6004u
 ibs      300.3952p   -2.0454n -853.1730f
 ibd       12.6989p.  -2.3228n   -2.0441n
 vgs       -1.8033     3.4127     5.0000
 vds        3.1967   216.0402m    1.5873
 vbs        3.1967    -1.5873     0.
 vth        1.5227     1.0621   752.7939m
 vdsat     -2.7697     1.7056     3.6286
 beta      33.9589u  354.1125u   31.0878u
 gam eff  934.4466m  274.9837m  266.6896m
 gm        83.0102u   57.2975u   40.8057u
 gds      284.9798n  692.9529u   76.6201u
 gmb       21.5555u    5.8823u    6.4345u
 cdtot     19.6398f   13.4659f   14.5307f
 cgtot     10.6359f   14.4214f   20.3406f
 cstot     10.5045f   14.1456f   19.4636f
 cbtot     21.2558f    8.7829f    9.6333f
 cgs        2.0598f    7.2252f   11.1242f
 cgd        7.7025f    6.7958f    7.8410f


        ***** job concluded
******  Star-HSPICE  --     97.1   (970317) 15:10:36  98/08/14    solaris
******
: test: t-n t-p t-cd t-tox t-load 5v
 ******  job statistics summary           tnom   25.000 temp= 125.000
******

          total memory used        459 kbytes

 # nodes =     10 # elements=      4
 # diodes=      0 # bjts    =      0 # jfets   =      0 # mosfets =      3

    analysis       time      # points  tot. iter  conv.iter

    op point          0.02         1         14
    readin            0.59
    errchk            0.10
    setup             0.01
    output            0.00
          total cpu time          0.72 seconds
              job started at  15:10:36  98/08/14
              job ended   at  15:10:37  98/08/14
```

test.out

```
element  0:vcc
 volts      5.0000
 current -243.5362u
 power      1.2177m



    total voltage source power dissipation=    1.2177m       watts


**** mosfets


subckt
element  0:m1        0:m2        0:m3
model    0:phv.2     0:nmos.1    0:nmos.2
 id       243.5362u   243.5362u   243.5362u
 ibs      540.3528f  -15.4004f  -9.919e-18
 ibd       34.3366f  -17.4944f  -15.3854f
 vgs       -1.7499     3.4605      5.0000
 vds        3.2501   210.4074m     1.5395
 vbs        3.2501    -1.5395      0.
 vth       -1.3370     1.0577    752.8484m
 vdsat     -2.8063     1.6143      3.5863
 beta      47.7119u   543.6186u    47.9256u
 gam eff  955.9372m   278.4061m   266.6525m
 gm       117.9765u    83.3528u    60.5252u
 gds      698.1676n     1.0464m   118.8510u
 gmb       31.3449u     8.7740u     9.6939u
 cdtot     18.8145f    13.4336f    14.6278f
 cgtot     11.0620f    14.4226f    20.3701f
 cstot     10.9320f    14.0931f    19.2056f
 cbtot     20.4317f     8.6719f     9.3442f
 cgs        2.5600f     7.2140f    11.0765f
 cgd        7.6283f     6.8084f     7.9201f



        ***** job concluded
******  Star-HSPICE  --     97.1    (970317) 15:38:05  98/08/14    solaris

******
: test: t-n t-p t-cd t-tox t-load 5v

 ******  job statistics summary           tnom=  25.000 temp=  25.000

******

       total memory used        450 kbytes

 # nodes =     10 # elements=      4
 # diodes=      0 # bjts    =      0 # jfets   =      0 # mosfets =      3

    analysis      time      # points  tot. iter  conv.iter
    op point          0.02          1         14
    readin            0.59
    errchk            0.10
    setup             0.01
    output            0.00
          total cpu time          0.72 seconds
              job started at  15:38:05  98/08/14
              job ended   at  15:38:06  98/08/14


    the following time statistics are already included in the analysis time
    load              0.00
    solver            0.00
# external nodes =     4 # internal nodes =     6
# branch currents=     1 total matrix size=    11
    pivot based and non pivoting solution times
      non pivotting:  ----  decompose       0.00  solve           0.00
    matrix size(    39) = initial size(    38) + fill(     1)
    words copied=           0
lic: Release  token(s)
HSPICE job test.filter completed.
Fri Aug 14 15:38:06 PDT 1998
Fri Aug 14 15:38:06 PDT 1998
```

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