Termination of the V_{PP} and Mode Pin for RH1020 and RH1280 Devices in a Radiation Environment

There is a concern about the use of Actel RH1020 or RH1280 Field Programmable Gate Arrays (FPGA) in a space-flight, radiation-environment with the MODE and/or V_{PP} pins left unterminated. It is trivial to show that the MODE pin must be terminated to GND. The effects of a floating V_{PP} pin are more difficult to definitively assess. The conclusion is that the V_{PP} pin must be properly terminated for reliable operation of the device.

MODE Pin

The MODE pin is used to control both the state of the device (e.g., normal, programming, debug, outputs disabled, various test modes, etc.) and the operation with regular logic levels. The device can be put into various modes; when the MODE pin is in the logic one state, commands can be shifted into the internal registers via DCLK (Data Clock) and SDI (Serial Data In) and through proper sequencing. When the MODE pin is in the logic zero state, all of the mode registers and control path flip-flops are directly held in the inactive state, guaranteeing that the device is in normal operating mode. Note that there is no guarantee as to the states of these "configuration" registers at power-up.

The effects of a floating MODE pin are difficult to predict because almost anything can happen. For example, one state that the device might go into is to support board level test. In this mode, all of the device outputs are tristated. Other examples of possible modes include programming mode and various device test modes. Incorrect configuration can result in functional failures and/or high currents which may either damage or pose a serious reliability hazard to the hardware. The effects for damage to the device and the board must be assessed on a specific basis.

Testing has shown that when the MODE pin was tied high, it was quite easy to "latch-up" the device with heavy ions. The devices repeatedly drew excessive amounts of current. The probability of having a problem with an unterminated MODE pin is quite high.

The recommendations for the MODE pin is to terminate it to GND with a hard jumper in parallel with a 10k Ω resistor. The hard jumper protects against resistor failure. During the prototyping and debug stage the hard jumper can be removed and the Silicon Explorer probing capability can be utilized. The termination of the MODE pin for each Actel device on the flight board should be verified with an ohm meter. Programming the security/probe fuse does not eliminate the need to terminate the mode pin.

V_{PP} Pin

The V_{PP} pin is the input supply pin used for device programming (the *Radiation-Hardened FPGAs*' data sheet refers to pin 22 on the RH1020 and pin 107 on the RH1280 as V_{CC}). It is NOT RECOMMENDED to leave V_{PP} floating, since it may bounce around and a high voltage might put the device in programming mode. For operating in a radiation environment, there is a concern that unterminated leads can charge up. In various radiation cases this effect has been observed.

Under normal operating conditions (MODE low and V_{PP} high), the V_{PP} signal is used to bias transistors in the peripheral control circuitry of the FPGA and does not directly access the user-defined logic modules or fuses in the array core. When the device is in programming mode (MODE pin high), the V_{PP} signal can reach every module in the array core. If the MODE pin is not properly terminated, there is a risk that the device could be put into programming mode and all functionality would be lost. If MODE is tied low and V_{PP} is not properly terminated, then there is risk of damage to the peripheral control circuitry of the gate array.

The V_{PP} pin is designed to receive voltages exceeding V_{CC}. Under normal operating conditions, the V_{PP} signal is used to bias a high voltage FET along with the drain of that FET. The FET would break down at lower bias voltages. Various tests and analyses showed that in the radiation environment, a single ion was capable of rupturing an antifuse at 5 VDC, which corresponds to an electric field strength of approximately 6 MV/cm. Factors for rupture will include electric field strength, oxide quality and uniformity, and any parasitic junctions that may be biased.

Internally, a diode exists between the V_{CC} and V_{PP} signal. Under normal operating conditions (V_{PP} tied high), this diode cannot be forward-biased and the device will draw normal operating current as outlined in the *Actel FPGA Data Book*. If this diode becomes forward biased (a potential risk if V_{PP} floats and gets driven low), the device will draw excessive current. Also, we have found that the V_{PP} pin is the most sensitive pin to ESD on the RH1020 and RH1280.

It is recommended that the V_{PP} pin be directly connected to V_{CC}. Additionally, it should be verified with an ohm meter that the V_{PP} pins on all flight devices are properly terminated.

Conclusion

The above summary and discussion shows the effects of unterminated MODE and/or V_{PP} pins for Actel RH1020 and RH1280 devices relative to spaceflight use. It is trivial to show that the MODE pin must be grounded and this must be done and verified. The unterminated V_{PP} pin is more difficult to definitively assess because of the occurrence of a number of plausible failure scenarios. V_{PP} must be connected to V_{CC} directly.

When operating outside of a space environment, these pins must also be terminated to ensure proper configuration of the device operation.

Actel will not guarantee the long-term reliability of devices that were not always in a legal operating configuration. No credible analysis has been performed that would guarantee reliable operation of parts that were not always in a legal operating configuration.

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