Total Dose and SEE of Metal-To-Metal Antifuse FPGA

J. J. Wang[1], Brian Cronquist[1], John McCollum[1], Frank Hawley[1], Donald Yu[1], Richard Chan[1], Rich Katz[2], and Igor Kleyner[3]
[1]Actel Corporation, Sunnyvale, CA 94086
[2]NASA/GSFC, Greenbelt, MD 20771
[3]Orbital Sciences Corporation, Greenbelt, MD 20771

Abstract

The total dose effects and SEEs of RT54SX, a new radiation tolerant antifuse FPGA family, are presented. This device family employs a metal-to-metal antifuse technology and a sea-of-modules architecture. Devices manufactured by both 0.6 µm and 0.25 µm technology levels are tested. The devices demonstrate the total dose tolerance better than 100 krad(Si). They are SEL and SEDR immune. For SEU, 0.6 µm has LET_{th} of 12 MeV-cm^2/mg and cross section of 2 x 10^{-6} cm^2, and 0.25 µm has a lower LET_{th} but approximately the same cross section. Total dose hardening and SEU hardening are also investigated.

I. RT54SX

The RT54SX family is the subset of the Actel 54SX family of products. It has enhanced radiation performance for total dose effects and SEEs (single event effects). The present RT54SX family uses 0.6 and 0.25 µm CMOS technologies. The power supply compatibility for 0.6 µm is 3.3/5.0 V, and for 0.25 µm is 2.5/3.3/5.0 V. A brief introduction of the 54SX device is presented in this section.

A. Architecture and Basic Logic Modules

Figure 1 shows the "Sea-of-Module" architecture of the device. The logic module tiles are built underneath the interconnection routing tracks. Compared to the channeled architecture employed in the ONO antifuse FPGA, the area is drastically reduced. The reduction in area improves both the cost and performance.

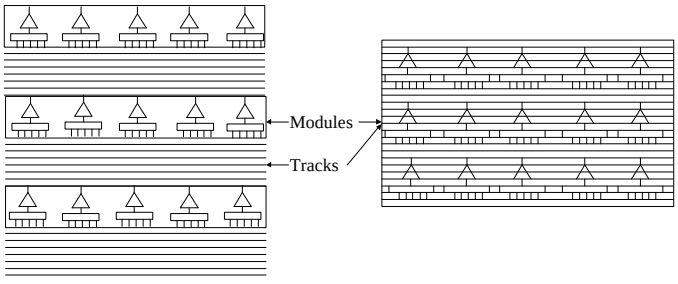

Figure 1. The Sea-of-Module architecture (right) uses less area than the channeled architecture (left).

Figure 2 shows the two basic logic modules in the device, the combinatorial cell (C-cell) and the register cell (R-cell). A C-cell can implement up to 5-input combinatorial functions. The R-cell (register cell) is basically a dedicated flip-flop (FF) with many control signals. These basic logic modules have the same circuit designs for either the 0.6 µm or 0.25 µm devices. Their layouts in the smaller feature technology basically have the same shape, only the size was shrunk.

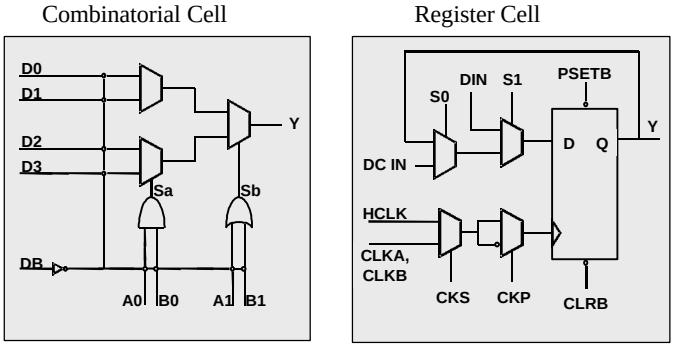

Figure 2. There are two basic logic modules in 54SX devices, the combinatorial logic module and register module.

B. Metal-to-Metal Antifuse

The antifuse switch is constructed between two metals, the so-called metal-to-metal antifuse. Figure 3 shows its structure. The antifuse material is composed of layers of amorphous silicon and dielectrics. Here the antifuse is sandwiched between metal 3 (the top metal) and the via-plug which is used for connecting metal 2 to metal 3. The antifuse size is basically defined by the via size. The smaller via size of technology-advancement/feature-size-shrinking can reduce the antifuse size, and subsequently the interconnect capacitance. The speed improvement can thus keep pace with the standard CMOS process. Actually, this is one of the major reasons to migrate from ONO to metal-to-metal technology. Metal-to-metal also has a lower programmed resistance (of approximately 25 ohms), which further improves the performance of a user's design.

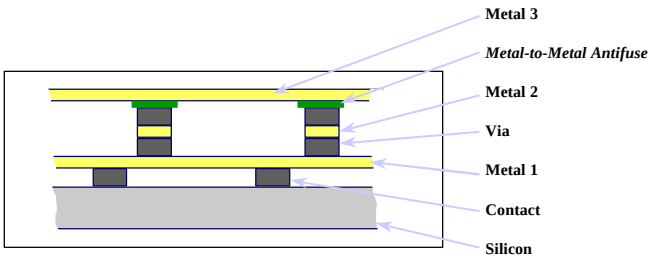

Figure 3. The Metal-to-Metal antifuse is formed between the top metal (metal 3 in this case) and the underneath plug via.

II. TOTAL DOSE EFFECTS

The total ionizing dose (TID) tolerance of both the 0.6 µm and 0.25 µm was evaluated. Process parameters relevant to TID were investigated. The limiting factor (parameter) for TID tolerance of the metal-to-metal antifuse FPGA is determined as static power supply leakage current (i.e. static I_{CC}), the same limiting factor as for the ONO antifuse device. In this paper, the tolerance is estimated by monitoring the static I_{CC} with total dose. Since the increment of static I_{CC} is larger for higher dose rate, the tolerance determined by the accelerated ground test is always conservative.

A. TID Tolerance of 0.6 µm Device

Figure 4 shows the TID tolerance of three process-split conditions. The static I_{CC} spec is 25 mA. Using this criterion and the worst case in each split, the tolerance is determined 70, 105, and 135 krad(Si) for each split condition respectively. The TID tolerance has to trade off with the programmability. Split condition to achieve 105 krad(Si) was selected for production.

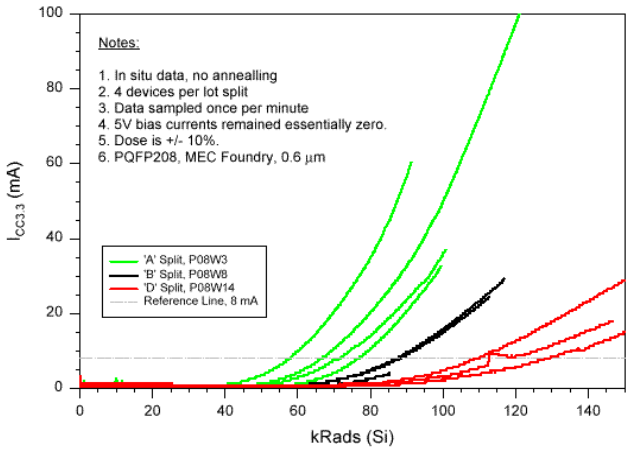

Figure 4. The static I_{CC} versus total dose for three process-split conditions of the 0.6 µm RT54SX16 device.

B. TID Tolerance of 0.25 µm Device

Figure 5 shows the tolerance of two process-split conditions. Only one device from each split condition was tested. Using the same 25 mA spec for static I_{CC}, the tolerance is determined as 90 and 230 krad(Si). The 0.25 µm device is the most advanced antifuse FPGA so far. The total dose effects on its AC/DC characteristics are not tested yet. Some new technologies employed for its fabrication, e.g. the shallow trench isolation, may impact the total dose effects differently from the traditional technologies. The present study is by no means conclusive. However, it gives a quick assessment of the potential of the new technology.

The reduction of the V_{CC} from 5.0 V to 3.3 V, and then to 2.5 V, apparently alleviated the leakage due to total dose effects. The increase of channel doping to combat the punch-through issue for the very short channel length also should contribute to the reduction of the leakage.

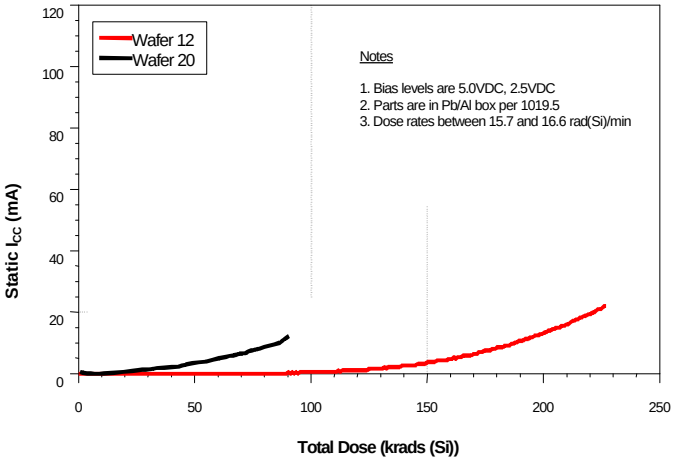

Figure 5. The static ICC versus total dose for two process-split conditions of the 0.25 µm RTSX prototype device.

III. SINGLE EVENT EFFECTS (SEE)

The SEE of the 0.6 and 0.25 µm RS54SX devices were evaluated by heavy ion bombardment. Table 1 lists the testing specifics. Proton tests were also performed on the 0.6 µm device at IUCF (Indiana University Cyclotron Facility).

Table 1 Heavy Ion Testing Specifics

Facility	BNL Tandem Van de Graaff		
Ion Species	Ti, Br, I, Au		
Fluence (per each run)	10^7 p/cm^2		
Flux	10^5 p/cm^2/sec		
Logic Design	Shift Register		
Signal Pattern	Checkerboard		
Signal Frequency	1 MHz		
DUT Bias	SEU	0.6 µm	5.0/3.3 V
		0.25 µm	3.3/2.5 V
	SEL or SEDR	0.6 µm	5.5/3.6 V
		0.25 µm	3.6/2.8 V
Temperature	Room		

A. SEL (Single Event Latchup) and SEDR (Single Event Dielectric Rupture)

The heavy ion test data show both 0.6 and 0.25 µm RTSX device are immune for SEL. No power supply current (I_{CC}) surge was ever detected using ions with LET up to 120 MeV-cm^2/mg. For comparison, SEL usually induces few hundreds mA of I_{CC} in the devices of similar size.

The test data also show both devices are immune to SEDR. SEDR can be detected by monitoring I_{CC} and switching off-and-on the power supply during testing to find if there is any permanent increase of I_{CC} due to heavy ion bombardment. For the worst case testing scenario, each DUT was oriented perpendicularly to the ion beam. As listed in table 1, ions as heavy as gold (LET of ~80 MeV-cm^2/mg) were used to detect SEDR.

B. SEU of 0.6 µm Device

Figure 6 shows the SEU data of the R-cell. The data fit into a Weibull distribution with a relatively large width and a small shape. This is consistent with the characteristics of the R-cell design, in which each storage node has several active junctions with different threshold LETs.

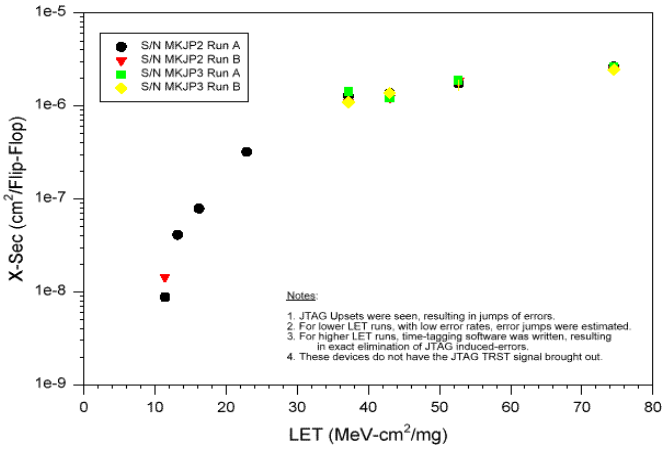

Figure 6. 0.6 µm RT54SX16 SEU data.

A checkerboard signal input was used for the detection of the errors due to SET (single event transient) in the clock network. The delay of the error count by computer and its display system is much longer than the cycle time of the shift register (1 µs). The error count due to clock-SET would be massive, as large as the total number of bits of the shift register on the computer screen. During the present testing, the increments of errors were small single digital numbers, indicating that there were no errors induced by the clock-SET.

The LET threshold is approximately 12 MeV-cm^2/mg, below the number (15 MeV-cm^2/mg) generally believed to be needed for the immunity of the SEU induced by a proton. Proton-induced SEU tests were done at IUCF. One energy, 193MeV was used. The DUT was biased at 5.0/3.3V and irradiated at room temperature. The total fluence for each run was 1.6 x 10^{12} p/cm^2 by using a flux of 1 x 10^9 p/cm^2/sec. The same design pattern and signal input as those for the heavy-ion testing were used. The results show the saturation cross section as 6.3 x 10^{-15} cm^2 (at 193 MeV). This slight sensitivity to proton SEU was further investigated by the upset rate prediction, which was performed by using a CRÈME-based simulator (Space Radiation 4.0). For a typical polar orbit, the upset rate was predicted to be dominated by the heavy ions (~80%).

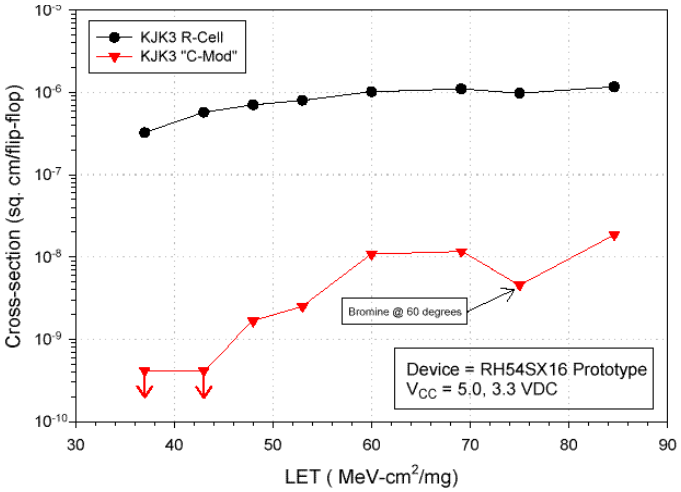

Figure 7. SEU data for FF constructed from one R-cell and two C-cells. The measurement is done on the 0.6 µm RH product from LMFS foundry, however the 0.6 µm RT product should have the same results.

There are two avenues to reduce the SEU error rate in the device. Instead of using the dedicated R-cell for constructing the flip-flop (FF), it is possible to construct a FF by using two C-cells. Shift registers made of C-cell FFs were tested for heavy ion SEUs. The results (Figure 7) show the C-cell FF has LET threshold greater than 43 MeV-cm^2/mg. In this Figure, shift register types made of C-cells and R-cells were tested simultaneously. A single FPGA device was programmed with both types of shift registers. The cross section of the C-cell FF is also significantly (two orders of magnitude) smaller than that of the R-cell's.

The other approach is to design an SEU-hardened R-cell. A triple-module-redundant design is to be implemented. The SEU hardness of this design is limited by the single-strike multiple-bit-upset mechanism [1,2]. The upset rate was predicted from simulated results using Space Radiation 4.0. In a GEO environment, the error rate for this hardened R-cell was predicted below 1 x 10^{-10} upset/bit/day.

Possible soft errors caused by single event transients in the combinational logic were also investigated. SPICE simulations using the critical charge concept were performed. The results show that the threshold LET is >50 MeV-cm^2/mg. To be more specific, ions with LETs less than this threshold

will not induce a transient strong enough to propagate through the net and reach a storage element in the device.

C. SEU of 0.25 µm Device

Figure 8 shows the results for both R-cell and C-cell FFs. These data were taken on pre-production devices. Nevertheless, they have the same memory cell designs as the production devices. The data indicate that the 0.25 µm device is more vulnerable than 0.6 µm to heavy-ions SEU. Compared the SEU of C-cell FFs, 0.25 µm has a lower LET threshold and larger saturation cross section.

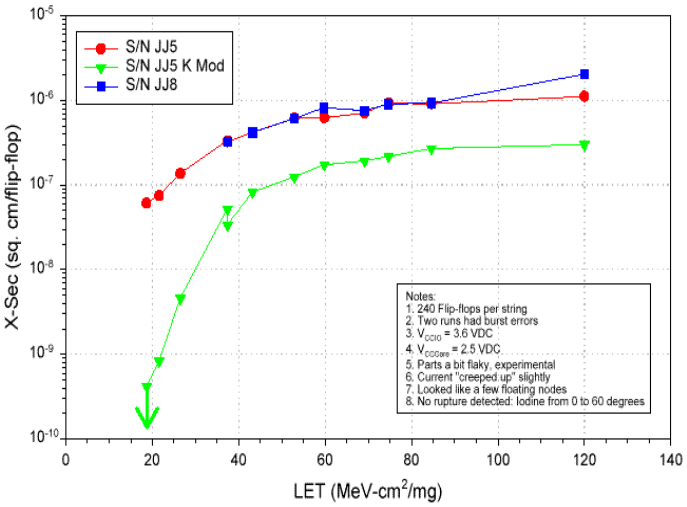

Figure 8. Preliminary SEU data of 0.25 µm RT54SX32. The top two curves are measured from R-cell FF, the bottom curve from C-cell FF.

The increased SEU sensitivity cannot be simply explained by the shrinking of the feature size. In the layout, the same type of FF in 0.25 µm is approximately one quarter the size as in 0.6 µm. But the resulted saturation cross section is about the same in them. However at least one trend is clear, the reduction of the power supply voltage (Vcc) from 5.0/3.3 V to 3.3/2.5 V will definitely increase the SEU sensitivity.

IV. CONCLUSIONS

The metal-to-metal antifuse FPGA is so far the best radiation-tolerant FPGA device. It has the intrinsic radiation immune programmable switch. Its total dose tolerance can be improved to over 100 krad(Si). It is SEL and SEDR immune. In other words, no permanent damage mechanisms exist in this device. SEU is also better than the previous ONO antifuse FPGA. However, the V_{CC} reduction due to the feature shrinking poses the greatest challenge for the future device SEU mitigation.

REFERENCES

[1] L. D. Edmonds, "A Distribution Function for Double-Bit Upsets," IEEE Trans. Nucl. Sci., 36, pp. 1344-1346, 1989.

[2] E. C. Smith and M. Shoga, "Double Upsets from Glancing Collisions: A Simple Model Verified with Flight Data," IEEE Trans. Nucl. Sci., 39, pp. 1859-1864, 1992.