54SX Family FPGAs

Leading Edge Performance

- 320 MHz Internal Performance
- 3.7 ns Clock-to-Out (Pin-to-Pin)
- 0.1 ns Input Set-Up
- 0.25 ns Clock Skew

Specifications

- 12,000 to 48,000 System Gates
- Up to 249 User-Programmable I/O Pins
- Up to 1080 Flip-Flops
- 0.35µ CMOS

Features

- 66 MHz PCI
- CPLD and FPGA Integration
- Single Chip Solution
- 100% Resource Utilization with 100% Pin Locking
- 3.3V Operation with 5.0V Input Tolerance
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

SX Product Profile

	A54SX08	A54SX16	A54SX16P	A54SX32
Capacity				
Typical Gates	8,000	16,000	16,000	32,000
System Gates	12,000	24,000	24,000	48,000
Logic Modules	768	1,452	1,452	2,880
Combinatorial Cells	512	924	924	1800
Register Cells (Dedicated Flip-Flops)	256	528	528	1,080
Maximum User I/Os	130	175	175	249
Clocks	3	3	3	3
JTAG	Yes	Yes	Yes	Yes
PCI	—	—	Yes	—
Clock-to-Out	3.7 ns	3.9 ns	4.4 ns	4.6 ns
Input Set-Up (External)	0.8 ns	0.5 ns	0.5 ns	0.1 ns
Speed Grades	Std, –1, –2, –3	Std, –1, –2, –3	Std, –1, –2, –3	Std, –1, –2, –3
Temperature Grades	C, I, M	C, I, M	C, I, M	C, I, M
Packages (by pin count)				
PLCC	84	—	—	—
PQFP	208	208	208	208
VQFP	100	100	100	—
TQFP	144, 176	176	144, 176	144, 176
PBGA	—	—	—	313, 329
FBGA	144	—	—	—

General Description

Actel's SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

Actel's SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hard-wired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX devices have easy-to-use I/O cells that do not require HDL instantiation, facilitating design re-use and reducing design and verification time.

Ordering Information

A54SX16 P – 2 PQ 208

Application (Temperature Range)
- Blank = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)
- M = Military (–55 to +125°C)
- PP = Pre-production

Package Lead Count

Package Type
- BG = Ball Grid Array
- PL = Plastic Leaded Chip Carrier
- PQ = Plastic Quad Flat Pack
- TQ = Thin (1.4 mm) Quad Flat Pack
- VQ = Very Thin (1.0 mm) Quad Flat Pack
- FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
- Blank = Standard Speed
- –1 = Approximately 15% Faster than Standard
- –2 = Approximately 25% Faster than Standard
- –3 = Approximately 35% Faster than Standard

- Blank = Not PCI Compliant
- P = PCI Compliant

Part Number
- A54SX08 = 12,000 System Gates
- A54SX16 = 24,000 System Gates
- A54SX16P = 24,000 System Gates
- A54SX32 = 48,000 System Gates

Product Plan

	Speed Grade*				Application		
	Std	–1	–2	–3	C	I†	M•
A54SX08 Device							
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	—
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	—
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	—
176-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	—
A54SX16 Device							
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	P
176-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	P
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	P
A54SX16P Device							
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	—
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	—
176-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	—
A54SX32 Device							
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	P
176-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	P
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	P
313-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔	✔	✔	—
329-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔	✔	✔	—

Contact your Actel sales representative for product availability.

Applications: *C = Commercial* *I = Industrial* *M = Military*

Availability: *✔ = Available* *P = Planned* *— = Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard* *–3 = Approx. 35% faster than Standard*

† Only Std, –1, –2 Speed Grade

• Only Std, –1 Speed Grade

Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	—	—	111
A54SX16	—	81	175	—	147	—	—	—
A54SX16P	—	81	175	113	147	—	—	—
A54SX32	—	—	174	113	147	249	249	—

Package Definitions *(Consult your local Actel sales representative for product availability.)*

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch (1.0 mm) Ball Grid Array

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

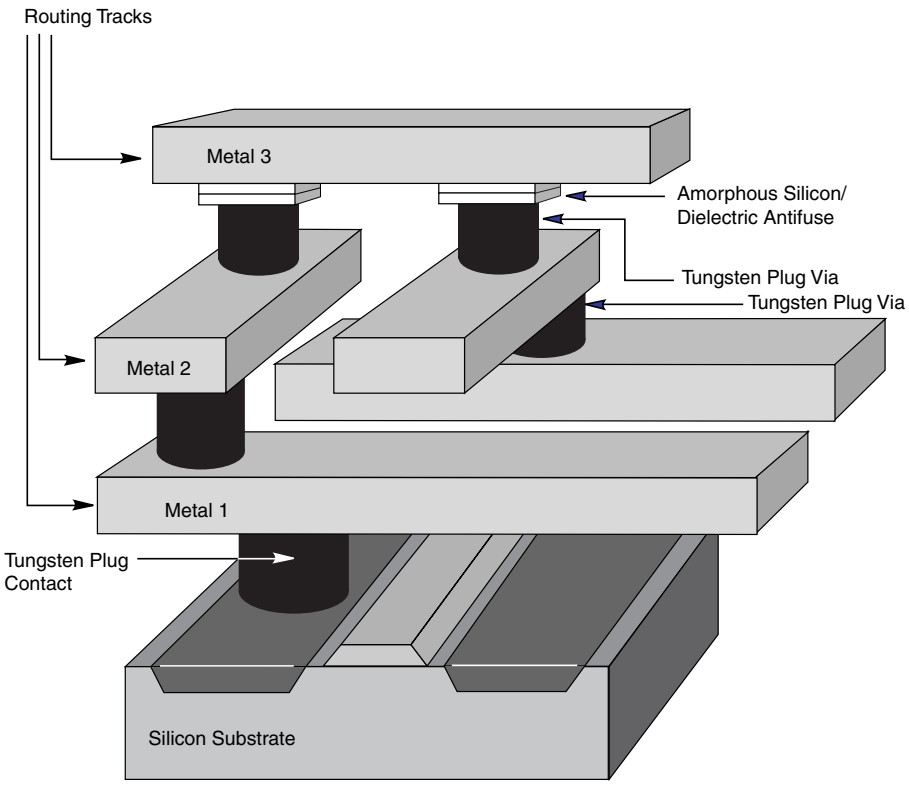


Figure 1 • *SX Family Interconnect Elements*

Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 2 on page 5). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

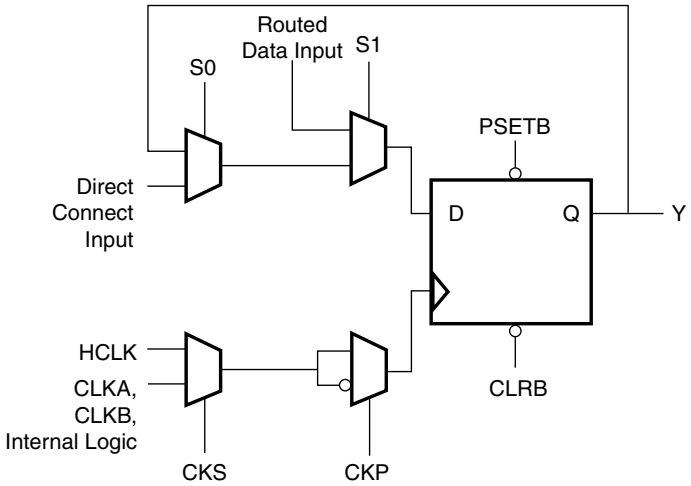


Figure 2 • R-Cell

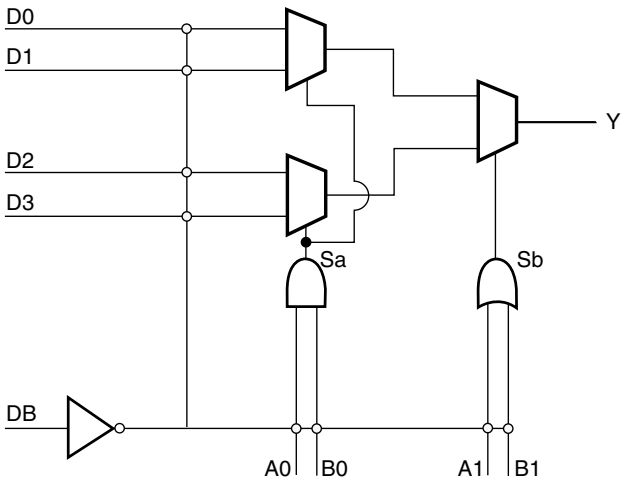


Figure 3 • C-Cell

Chip Architecture

The SX family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 4 on page 6). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

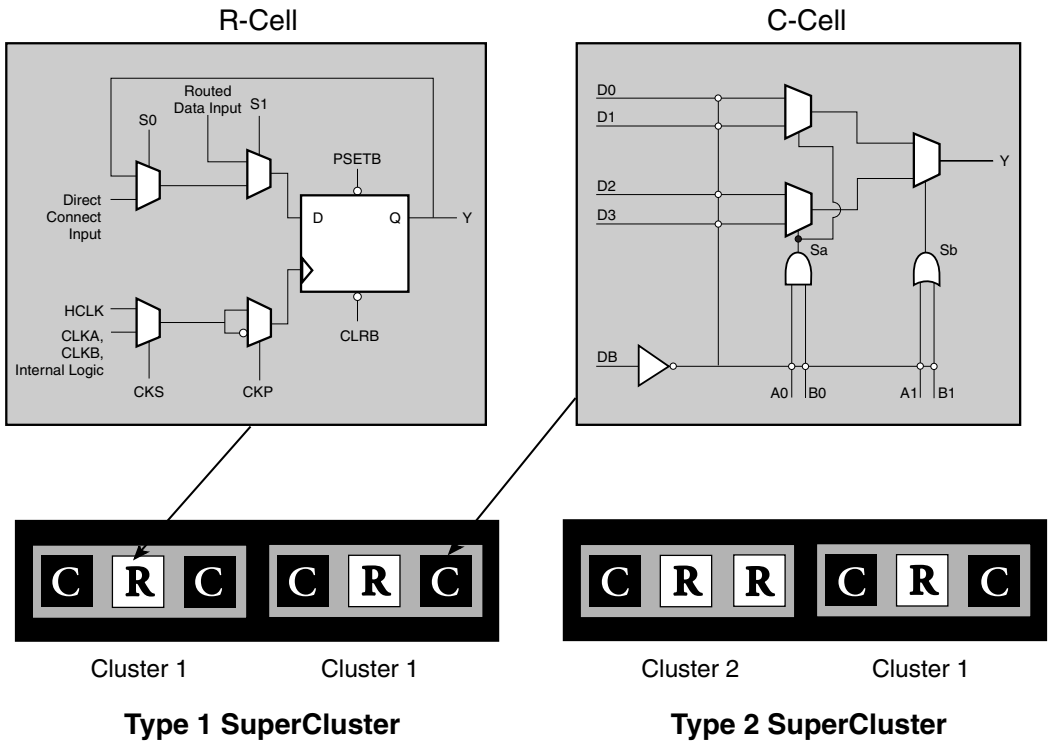


Figure 4 • *Cluster Organization*

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 5 and Figure 6 on page 7). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place and route software to minimize signal propagation delays.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hard wired from the HCLK buffer to the clock select MUX in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hard-wired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

Other Architectural Features

Technology

Actel's SX family is implemented on a high-voltage twin-well CMOS process using 0.35µ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25Ω with capacitance of 1.0 fF for low signal impedance.

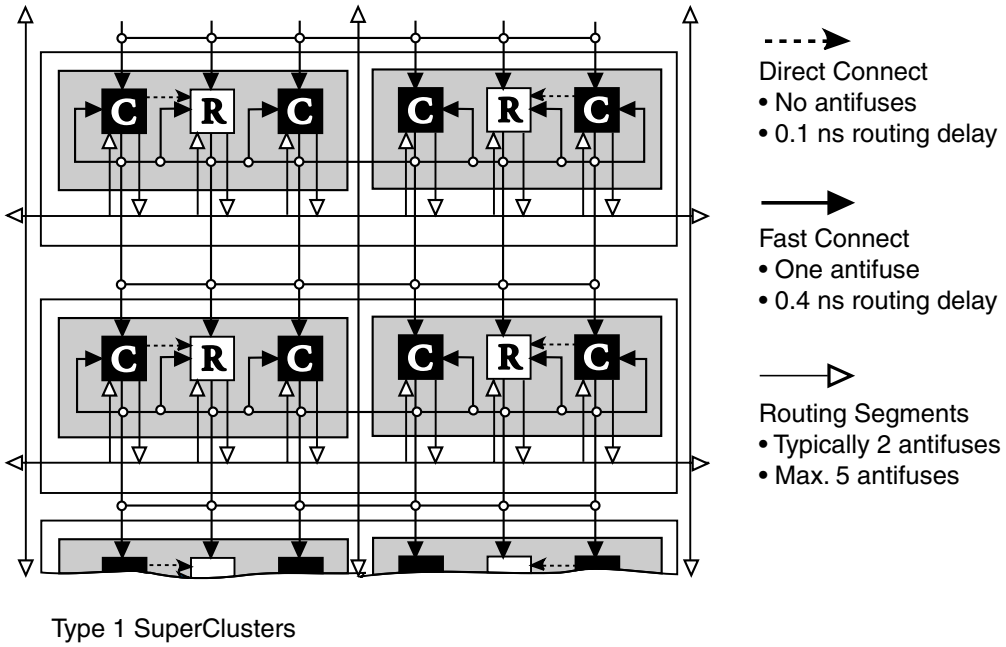


Figure 5 • *DirectConnect and FastConnect for Type 1 SuperClusters*

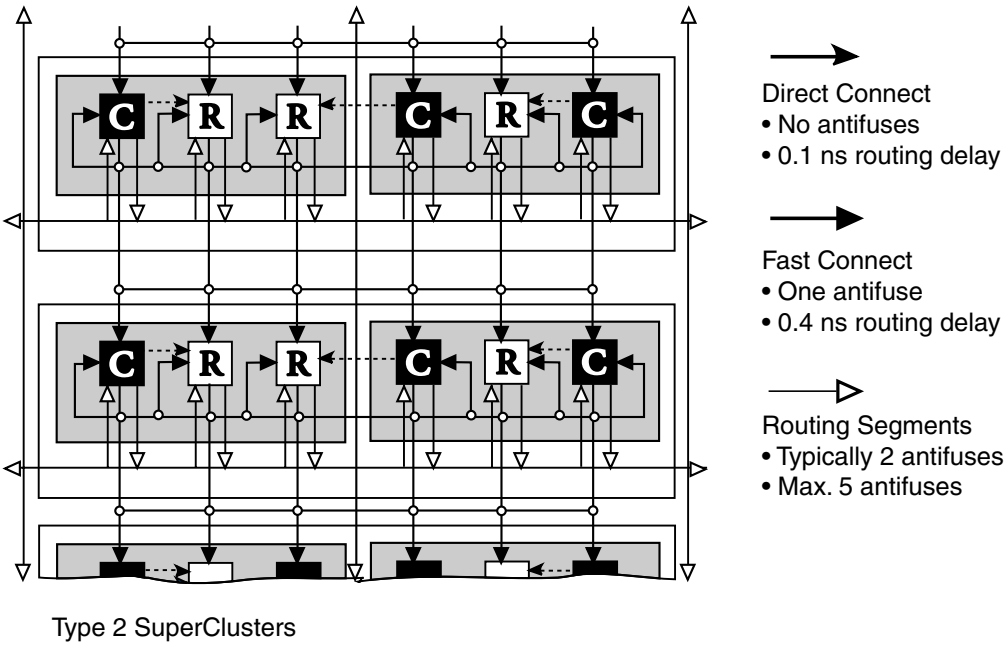


Figure 6 • *DirectConnect and FastConnect for Type 2 SuperClusters*

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place and route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The SX family supports 3.3V operation and is designed to tolerate 5.0V inputs. (Table 1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power architecture on the market.

Table 1 • *Supply Voltages*

	V_{CCA}	V_{CCI}	V_{CCR}	Input Tolerance	Output Drive
A54SX08 **A54SX16** **A54SX32**	3.3V	3.3V	5.0V	3.3V	3.3V
	3.3V	3.3V	5.0V	5.0V	3.3V
A54SX16P	3.3V	3.3V	3.3V	3.3V	3.3V
	3.3V	3.3V	5.0V	5.0V	3.3V
	3.3V	5.0V	5.0V	5.0V	5.0V

Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 2.In the dedicated test mode, TCK, TDI and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode. .

Table 2 • *Boundary Scan Pin Functionality*

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10k Ω on TMS

Development Tool Support

The SX devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage, Actel's suite of FPGA development point tools for PCs and Workstations, includes the ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and device programming software.

In addition, the SX devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to only a few seconds.

SX Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 7 illustrates the

interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification. The TRST pin is equipped with a pull-up resistor. To remove the boundary scan state machine from the reset state during probing, it is recommended that the TRST pin be left floating.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

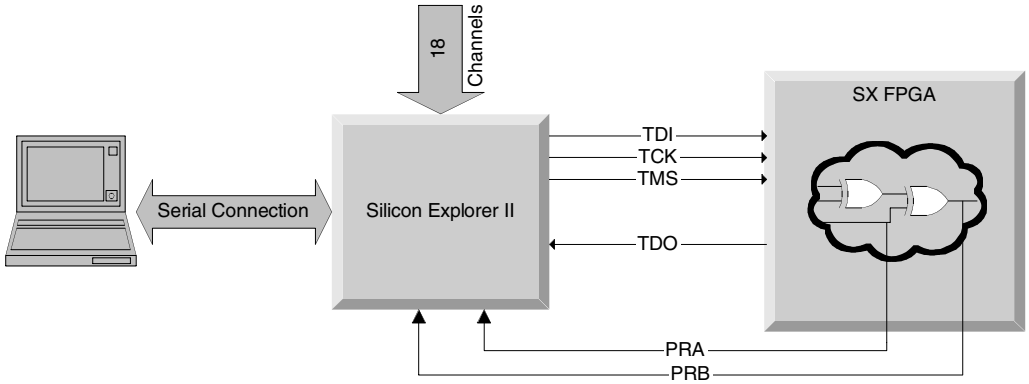


Figure 7 • *Probe Setup*

3.3V/5V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCR}[2]	DC Supply Voltage[3]	–0.3 to +6.0	V
V_{CCA}[2]	DC Supply Voltage	–0.3 to +4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to +4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX16P)	–0.3 to +6.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to +5.0	mA
T_{STG}	Storage Temperature	–40 to +125	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.*
3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward-bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to+70	–40 to +85	–55 to +125	°C
3.3V Power Supply Tolerance	±10	±10	±10	%V_{CC}
5.0V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = -20uA) (CMOS)	(V_{CCI} – 0.1)	V_{CCI}	(V_{CCI} – 0.1)	V_{CCI}	V
	(I_{OH} = -8mA) (TTL)	2.4	V_{CCI}			
	(I_{OH} = -6mA) (TTL)			2.4	V_{CCI}	
V_{OL}	(I_{OL}= 20uA) (CMOS)		0.10			V
	(I_{OL} = 12mA) (TTL)		0.50			
	(I_{OL} = 8mA) (TTL)				0.50	
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in 54SX Devices" on page 18.				

PCI Compliance for the 54SX Family

The 54SX family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

A54SX16P DC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		4.75	5.25	V
V_{CCI}	Supply Voltage for IOs		4.75	5.25	V
V_{IH}	Input High Voltage[1]		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

A54SX16P AC Specifications for (PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$[1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$[1, 2]	$–44 + (V_{OUT} – 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$[1, 3]		Equation A: on page 13	
	(Test Point)	$V_{OUT} = 3.1$[3]		–142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \ge 2.2$[1]	95		mA
		$2.2 > V_{OUT} > 0.55$[1]	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0$[1, 3]		Equation B: on page 13	mA
	(Test Point)	$V_{OUT} = 0.71$[3]		206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V to 2.4V load[4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V to 0.4V load[4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 8. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 8. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

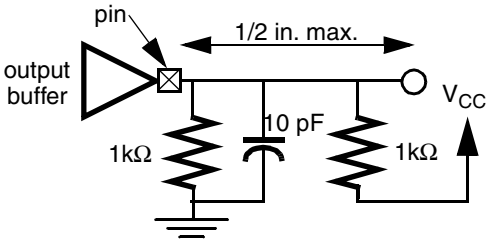


Figure 8 shows the 5.0V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P family.

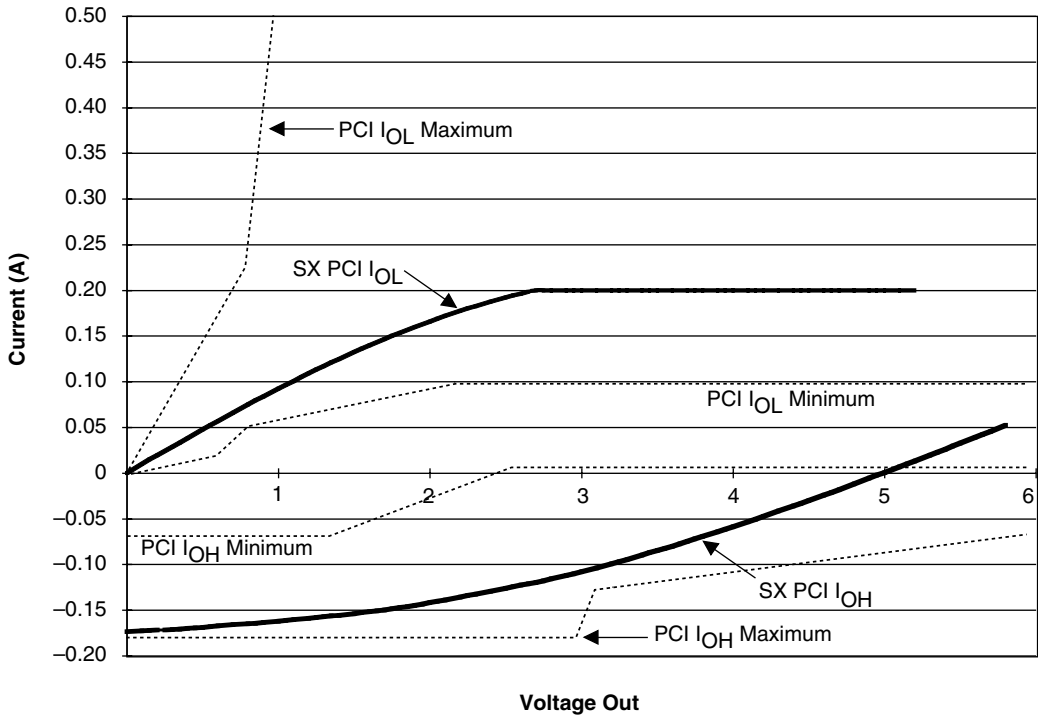


Figure 8 • *5.0V PCI Curve for A54SX16P Family*

Equation A:

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$
$$\text{for } V_{CC} > V_{OUT} > 3.1V$$

Equation B:

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.71V$$

A54SX16P DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for IOs		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CC}$		±10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10pF (except for CLK).*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

A 54SX16P AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
	Switching Current High	$0 < V_{OUT} \le 0.3V_{CC}$[1]			mA
		$0.3V_{CC} \le V_{OUT} < 0.9V_{CC}$[1]	$-12V_{CC}$		mA
$I_{OH(AC)}$		$0.7V_{CC} < V_{OUT} < V_{CC}$[1, 2]	$-17.1 + (V_{CC} - V_{OUT})$	Equation C: on page 16	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$[2]		$-32V_{CC}$	mA
	Switching Current High	$V_{CC} > V_{OUT} \ge 0.6V_{CC}$[1]			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$[1]	$16V_{CC}$		mA
$I_{OL(AC)}$		$0.18V_{CC} > V_{OUT} > 0$[1, 2]	$26.7V_{OUT}$	on page 16	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}$[2]		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \le -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate[3]	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$slew_F$	Output Fall Slew Rate[3]	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 9. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 9. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

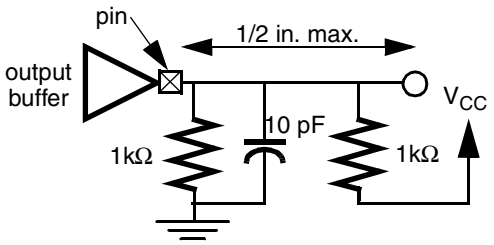


Figure 9 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P family.

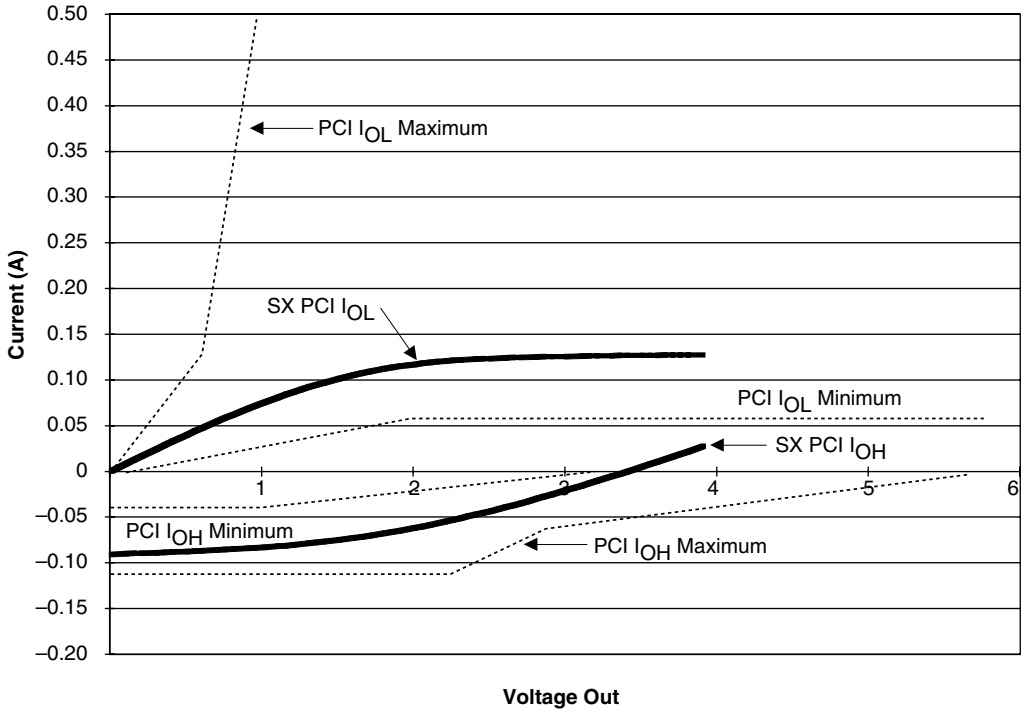


Figure 9 • *3.3V PCI Curve for A54SX16P Family*

Equation C:

$$I_{OH} = (98.0/V_{CC}) * (V_{OUT} - V_{CC}) * (V_{OUT} + 0.4V_{CC})$$
$$\text{for } V_{CC} > V_{OUT} > 0.7\ V_{CC}$$

Equation D:

$$I_{OL} = (256/V_{CC}) * V_{OUT} * (V_{CC} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\ V_{CC}$$

Power-Up Sequencing

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	Possible damage to device.
A54SX16P				
3.3V	3.3V	3.3V	3.3V Only	No possible damage to device.
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	Possible damage to device.
3.3V	5.0V	5.0V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Power-Down Sequencing

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3V	5.0V	3.3V	5.0V First 3.3V Second	Possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.
A54SX16P				
3.3V	3.3V	3.3V	3.3V Only	No possible damage to device.
3.3V	5.0V	3.3V	5.0V First 3.3V Second	Possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.
3.3V	5.0V	5.0V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Evaluating Power in 54SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

- Estimate the power consumption of the application.
- Calculate the maximum power allowed for the device and package.
- Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the 54SX family is the sum of the DC power dissipation and the AC power dissipation. Use Equation 1 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC} \quad (1)$$

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown below for commercial, worst case conditions (70°C).

Table 3 •

I_{CC}	V_{CC}	Power
4mA	3.6V	14.4mW

The DC power dissipation is defined in Equation 2 as follows:

$$P_{DC} = (I_{standby})*V_{CCA} + (I_{standby})*V_{CCR} + (I_{standby})*V_{CCI} + x*V_{OL}*I_{OL} + y*(V_{CCI} - V_{OH})*V_{OH} \quad (2)$$

AC Power Dissipation

The power dissipation of the 54SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance and power supply voltage. The AC power dissipation is defined as follows:

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer} \quad (3)$$

$$P_{AC} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{Module} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{RCLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{RCLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1}))_{HCLK}] \quad (4)$$

Definition of Terms Used in Formula

m	=	Number of logic modules switching at f_m
n	=	Number of input buffers switching at f_n
p	=	Number of output buffers switching at f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
x	=	Number of I/Os at logic low
y	=	Number of I/Os at logic high
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
s_1	=	Number of clock loads on the dedicated array clock
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_{EQHV}	=	Variable capacitance of dedicated array clock
C_{EQHF}	=	Fixed capacitance of dedicated array clock
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz
f_{s1}	=	Average dedicated array clock rate in MHz

	A54SX08	A54SX16	A54SX16P	A54SX32
C_{EQM} (pF)	4.0	4.0	4.0	4.0
C_{EQI} (pF)	3.4	3.4	3.4	3.4
C_{EQO} (pF)	4.7	4.7	4.7	4.7
C_{EQCR} (pF)	1.6	1.6	1.6	1.6
C_{EQHV}	0.615	0.615	0.615	0.615
C_{EQHF}	60	96	96	140
r_1 (pF)	87	138	138	171
r_2 (pF)	87	138	138	171

Guidelines for Calculating Power Consumption

The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follow:

Logic Modules (m)	=	20% of modules
Inputs Switching (n)	=	# inputs/4
Outputs Switching (p)	=	# output/4
First Routed Array Clock Loads (q_1)	=	20% of register cells
Second Routed Array Clock Loads (q_2)	=	20% of register cells
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	f/10
Average Input Switching Rate (f_n)	=	f/5
Average Output Switching Rate (f_p)	=	f/10
Average First Routed Array Clock Rate (f_{q1})	=	f/2
Average Second Routed Array Clock Rate (f_{q2})	=	f/2
Average Dedicated Array Clock Rate (f_{s1})	=	f
Dedicated Clock Array clock loads (s_1)	=	20% of regular modules

Sample Power Calculation

One of the designs used to characterize the A54SX family was a 528 bit serial in serial out shift register. The design utilized 100% of the dedicated flip-flops of an A54SX16P device. A pattern of 0101… was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101… caused 50% of the flip-flops to toggle from low to high at every clock cycle.

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the 54SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC} \text{ (dynamic power)} + P_{DC} \text{ (static power)} \quad (5)$$

AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer} \quad (6)$$

$$P_{AC} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{Module} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{RCLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{RCLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1}))_{HCLK}] \quad (7)$$

Step #1: Define Terms Used in Formula

V_{CCA}		3.3
Module		
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: f/10)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: f/5)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p(MHz) (Guidelines: f/10)	f_p	20
Output buffers buffer Capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.615
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step #2: Calculate Dynamic Power Consumption

$V_{CCA}*V_{CCA}$	10.89
$m*f_m*C_{EQM}$	0.02112
$n*f_n*C_{EQI}$	0.000136
$p*f_p*(C_{EQO}+C_L)$	0.000794
$0.5*(q_1*C_{EQCR}*f_{q1})+(r_1*f_{q1})$	0.11208
$0.5*(q_2*C_{EQCR}*f_{q2})+(r_2*f_{q2})$	0
$0.5*(s_1*C_{EQHV}*f_{s1})+(C_{EQHF}*f_{s1})$	0

P_{AC} = 1.461W

Step #3: Calculate DC Power Dissipation

DC Power Dissipation

$$P_{DC} = (I_{standby})*V_{CCA} + (I_{standby})*V_{CCR} + (I_{standby})*V_{CCI} + X*V_{OL}*I_{OL} + Y*(V_{CCI} - V_{OH})*V_{OH} \quad (8)$$

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby})*V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$P_{DC} = (I_{standby})*V_{CCA}$

P_{DC} = .55mA*3.3V

P_{DC} = 0.001815W

Step #4: Calculate Total Power Consumption

$P_{Total} = P_{AC} + P_{DC}$

P_{Total} = 1.461 + 0.001815

P_{Total} = 1.4628W

Step #5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46W. The characterized power consumption for this design at 200 MHz is 1.0164W. Figure 10 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

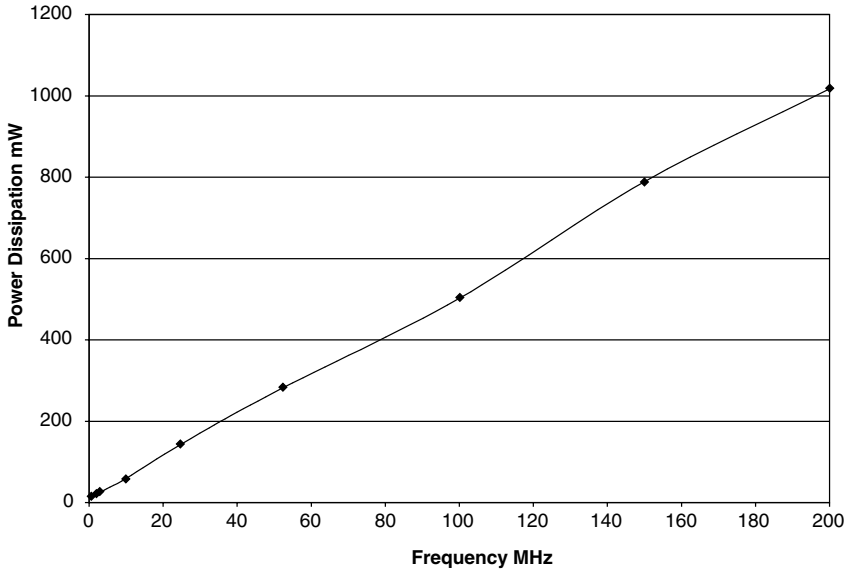


Figure 10 • *Power Dissipation*

Junction Temperature (T_J)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Package Thermal Characteristics section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

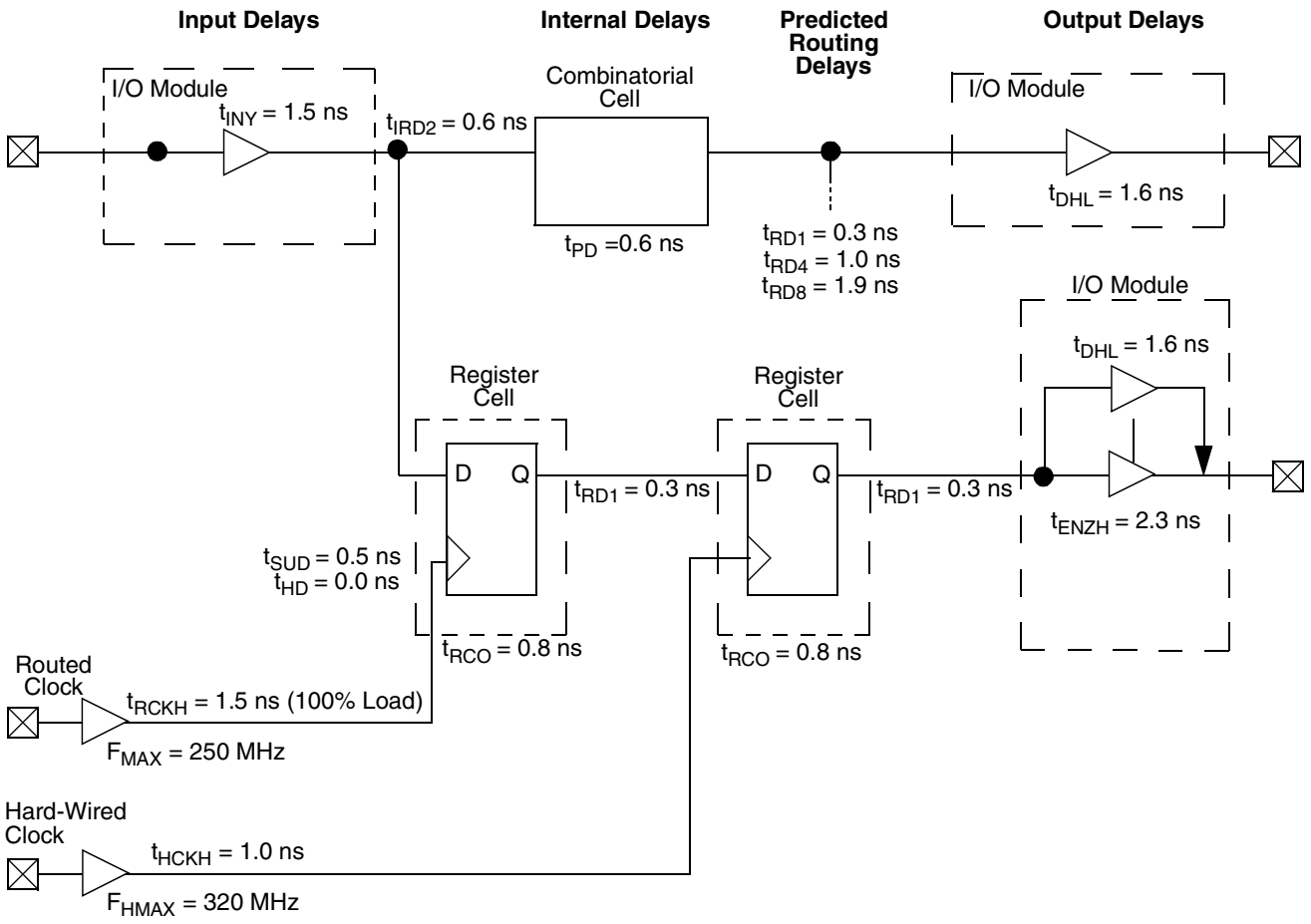
$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\ (\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{28\text{°C/W}} = 2.86\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note:

SX08 does not have a heat spreader.

54SX Timing Model*



**Values shown for A54SX08-3, worst-case commercial conditions.*

Hard-Wired Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$
= 1.5 + 0.3 + 0.5 – 1.0 = 1.3 ns

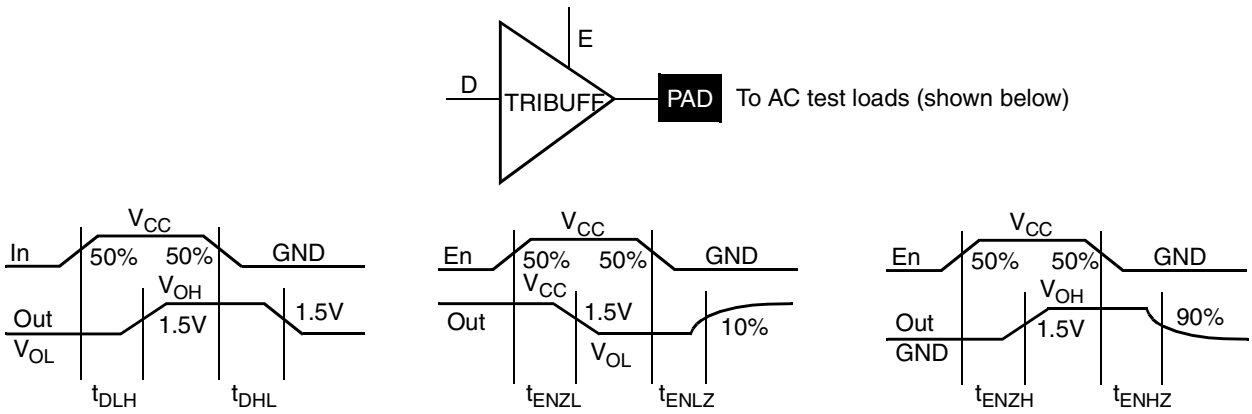
Clock-to-Out (Pin-to-Pin)
= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 ns

Routed Clock

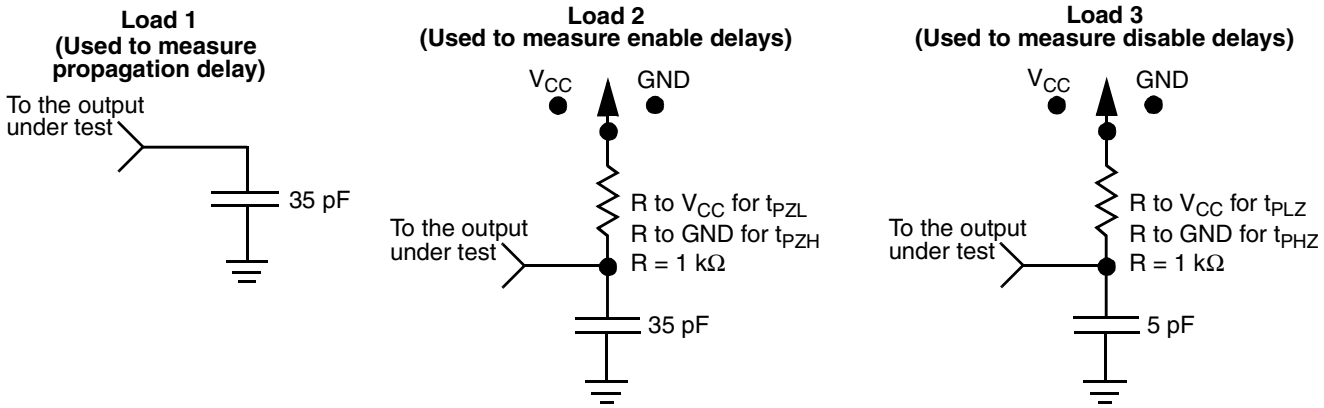
External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 1.5 + 0.3 + 0.5 – 1.5 = 0.8 ns

Clock-to-Out (Pin-to-Pin)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.52+ 0.8 + 0.3 + 1.6 = 4.2 ns

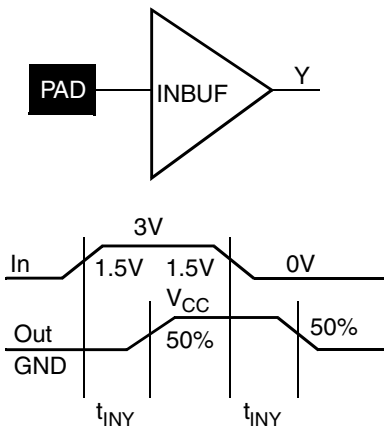
Output Buffer Delays



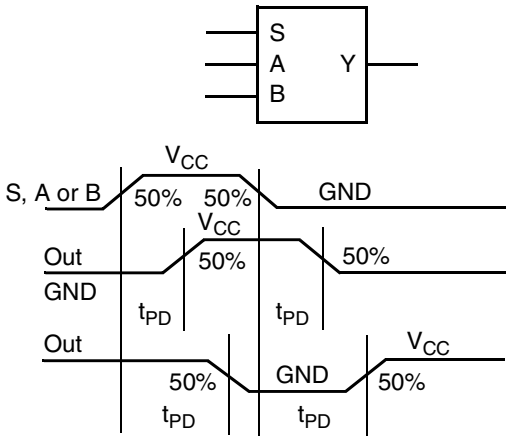
AC Test Loads



Input Buffer Delays

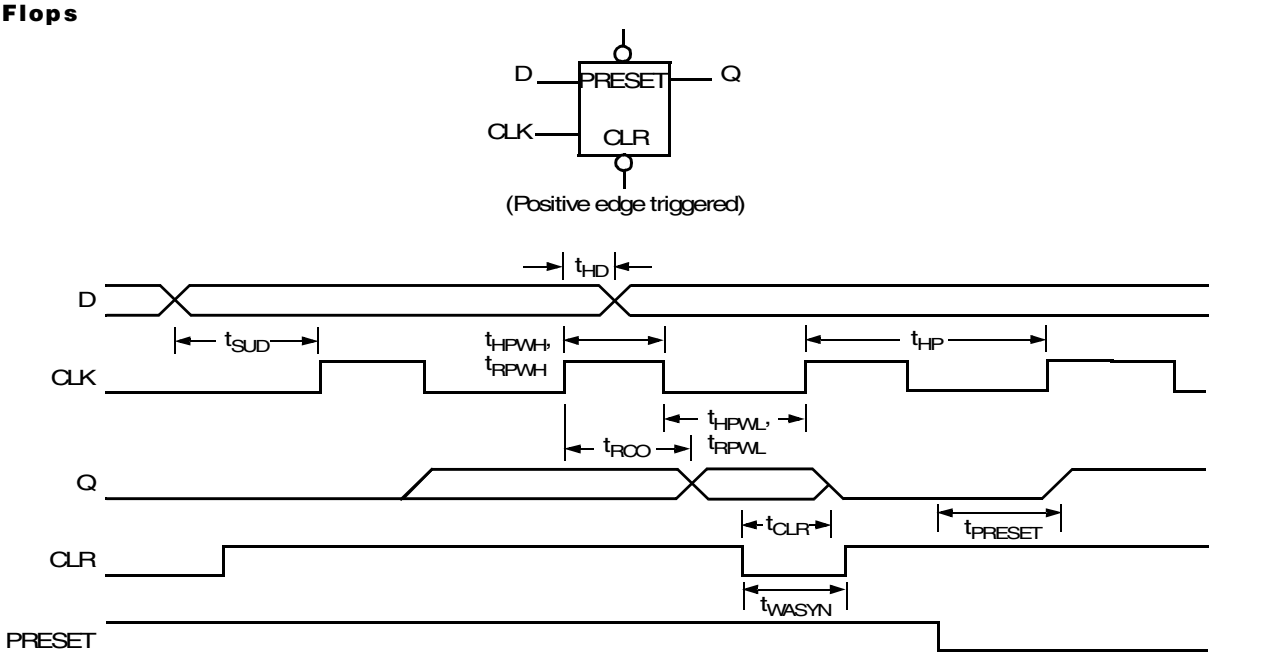


C-Cell Delays



Register Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for 54SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all 54SX family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the data sheet specifications section.

Timing Derating

54SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 3.0V)

	Junction Temperature (T_J)						
V_{CCA}	–55	–40	0	25	70	85	125
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

A54SX08 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR}= 4.75V, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX08 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.0		1.1		1.3		1.5	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.0		1.2		1.4		1.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.1		0.2		0.2		0.2	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.3		1.5		1.7		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.4		1.6		1.8		2.1	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.4		1.7		1.9		2.2	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.5		1.7		1.9		2.2	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.5		1.8		2.0		2.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.1		0.2		0.2		0.2	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4	ns
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.

A54SX16 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR}= 4.75V, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.4		1.5		1.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.2		1.4		1.6		1.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.8		2.1		2.5		2.8	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.8		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.5		0.5		0.5		0.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8	ns
TTL Output ModuleTiming[1]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.

A54SX16P Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR}= 4.75V, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.9		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	**Asynchronous Pulse Width**	**1.4**		**1.6**		**1.8**		**2.1**		**ns**
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16P Timing Characteristics (continued)

(Worst-Case Commercial Conditions, V_{CCR}= 4.75V, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.4		1.5		1.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.2		1.4		1.6		1.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.8		2.1		2.5		2.8	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.8		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.5		0.5		0.5		0.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8	ns
TTL Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		2.4		2.8		3.1		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.3		2.9		3.2		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.0		3.4		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.3		3.8		4.3		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.0		3.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.7		4.3	ns
TTL/PCI Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		1.5		1.7		2.0		2.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.9		2.2		2.4		2.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.6		3.0		3.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.1		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

A54SX16P Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CCR} = 3.0V, V_{CCA}, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
PCI Output Module Timing[1]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.8		2.0		2.3		2.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.7		2.0		2.2		2.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		0.8		1.0		1.1		1.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.2		1.2		1.5		1.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.0		1.1		1.3		1.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.1		1.3		1.5		1.7	ns
TTL Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		2.9		3.2		3.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.0		3.5		3.9		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.1		3.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

Note:

1. Delays based on 10 pF loading.

A54SX32 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR}= 4.75V, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{RD3}	FO=3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD8}	FO=8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{RD12}	FO=12 Routing Delay		4.0		4.7		5.3		6.2	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{IRD3}	FO=3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD4}	FO=4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD8}	FO=8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{IRD12}	FO=12 Routing Delay		4.0		4.7		5.3		6.2	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX32 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.9		2.1		2.4		2.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.9		2.1		2.4		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.4		2.7		3.0		3.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.4		2.7		3.1		3.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.7		3.0		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.7		3.1		3.6		4.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.7		3.1		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.8		3.2		3.6		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.85		0.98		1.1		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.23		1.4		1.6		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.30		1.5		1.7		2.0	ns
TTL Output Module Timing[1]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

Pin Description

CLKA/B Clock A and B

These pins are 3.3V/5.0V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

This pin is the 3.3V/5.0V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 2 on page 8). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 2 on page 8). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 2 on page 8). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 2 on page 8). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 1 on page 8.

V_{CCA} Supply Voltage

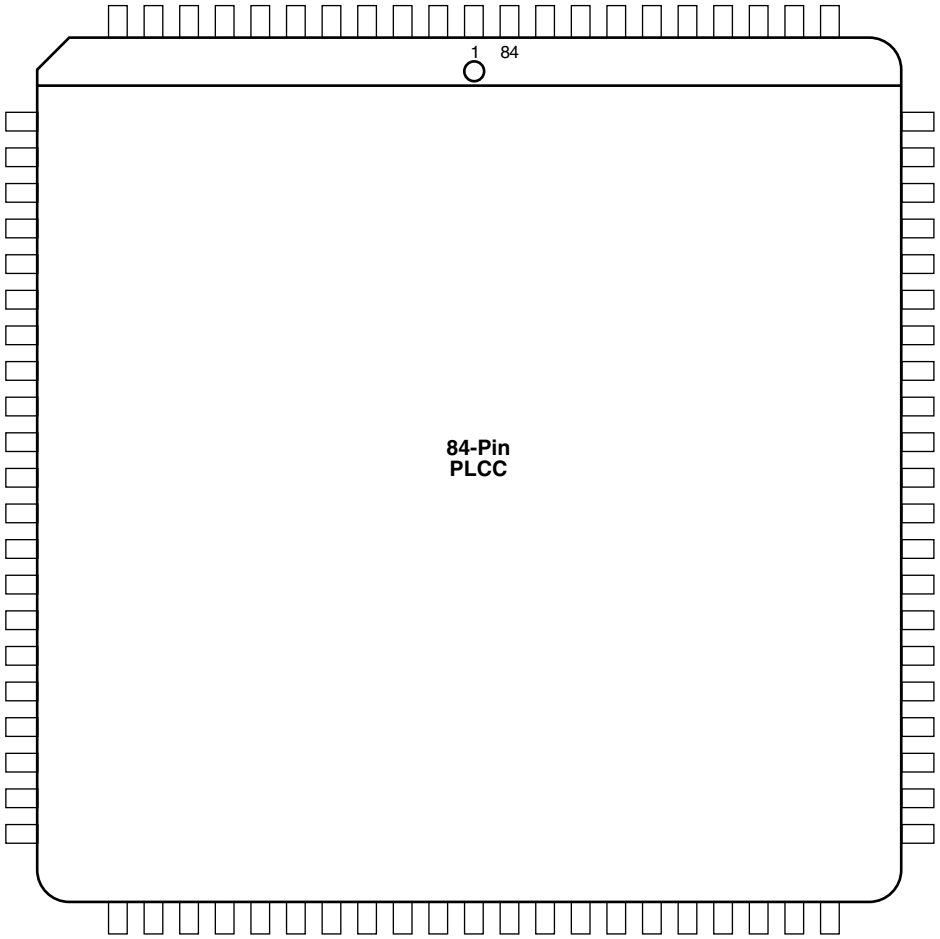
Supply voltage for Array. See Table 1 on page 8.

V_{CCR} Supply Voltage

Supply voltage for input tolerance (required for internal biasing) See Table 1 on page 8.

Package Pin Assignments

84-Pin PLCC (Top View)



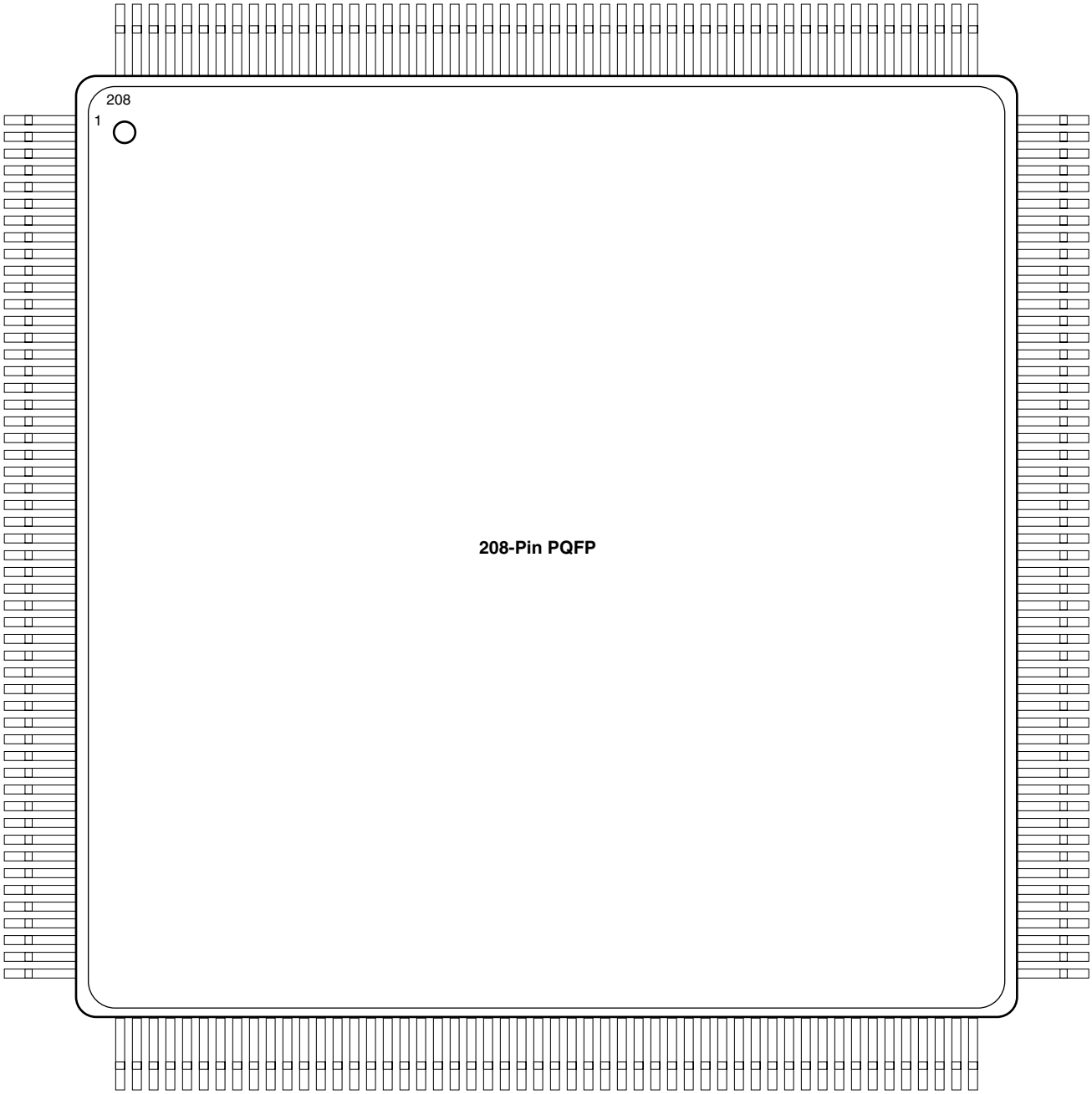
84-Pin PLCC Package

Pin Number	A54SX08 Function
1	V_{CCR}
2	GND
3	V_{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V_{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V_{CCA}
42	GND

Pin Number	A54SX08 Function
43	V_{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CCA}
60	V_{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V_{CCA}
69	GND
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

Package Pin Assignments (continued)

208-Pin PQFP (Top View)



208-Pin PQFP

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V_{CCR}	V_{CCR}	V_{CCR}
26	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND
80	V_{CCR}	V_{CCR}	V_{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O

** Please note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

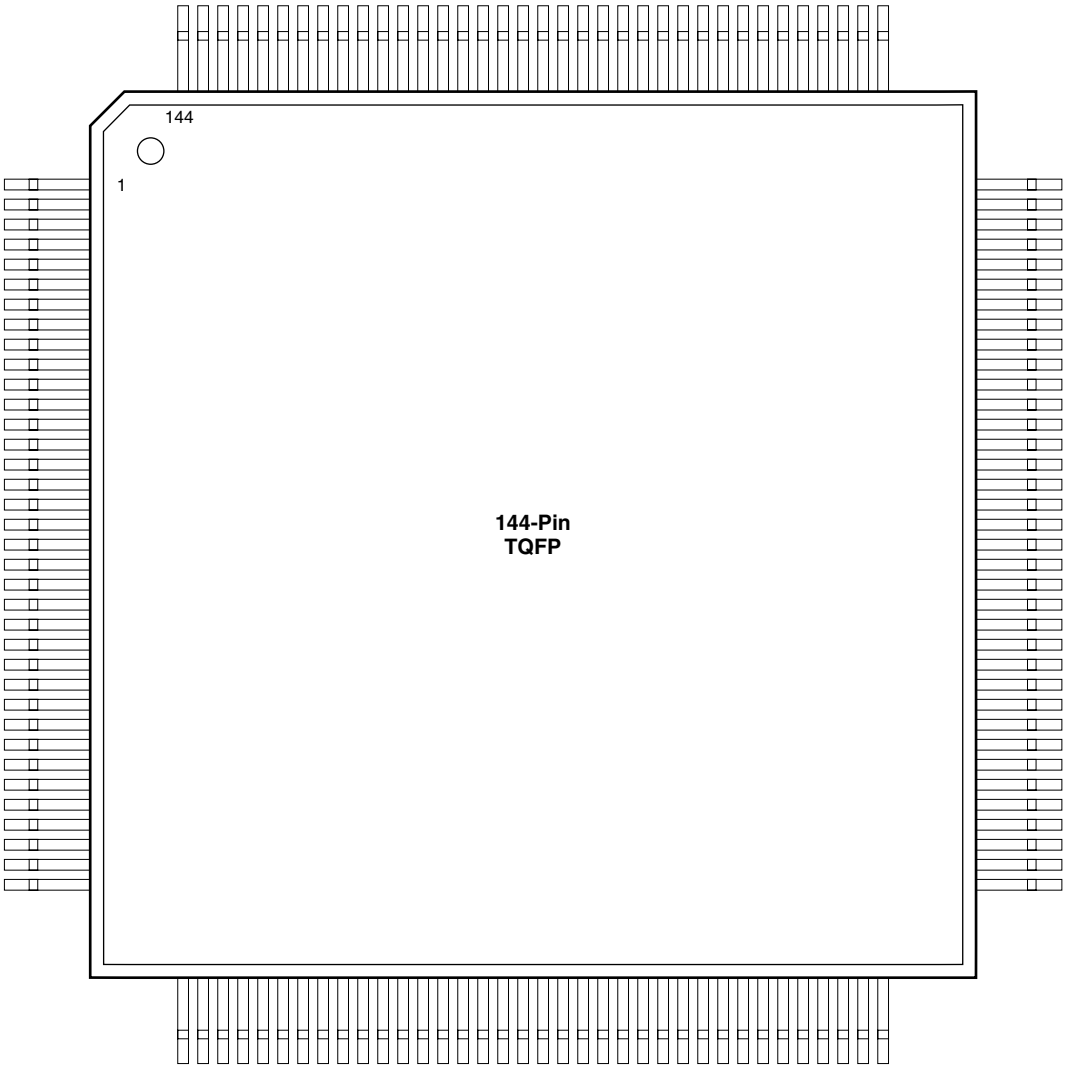
208-Pin PQFP (Continued)

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
107	I/O	I/O	I/O
108	NC	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND
132	V_{CCR}	V_{CCR}	V_{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O
145	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB
182	V_{CCR}	V_{CCR}	V_{CCR}
183	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

** Please note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

Package Pin Assignments (continued)

144-Pin TQFP (Top View)



144-Pin TQFP

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V_{CCI}	V_{CCI}	V_{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	V_{CCR}	V_{CCR}	V_{CCR}
20	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V_{CCI}	V_{CCI}	V_{CCI}
30	V_{CCA}	V_{CCA}	V_{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V_{CCA}	V_{CCA}	V_{CCA}
57	GND	GND	GND
58	V_{CCR}	V_{CCR}	V_{CCR}
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V_{CCI}	V_{CCI}	V_{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}

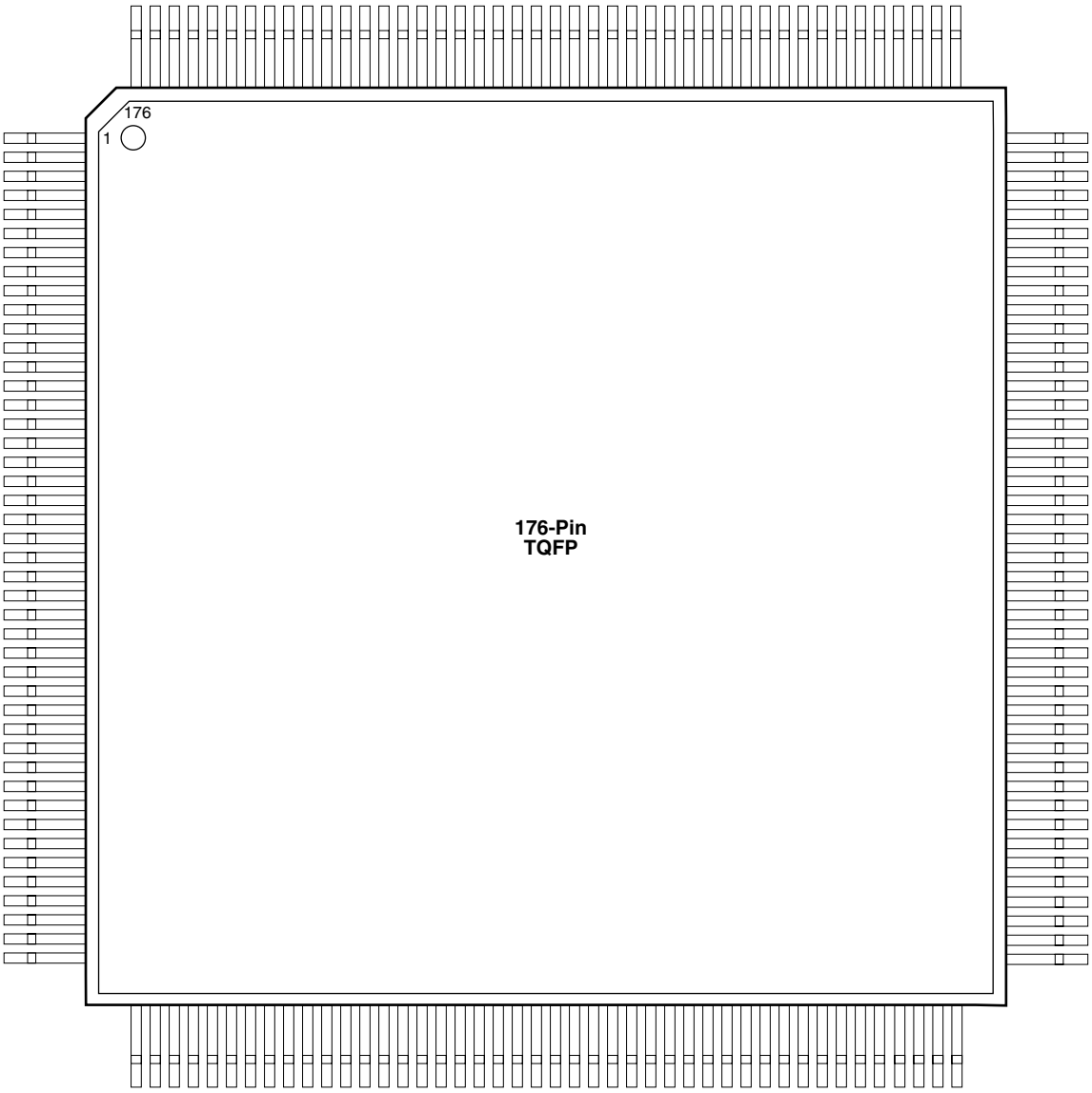
144-Pin TQFP (Continued)

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	V_{CCR}	V_{CCR}	V_{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V_{CCR}	V_{CCR}	V_{CCR}
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

176-Pin TQFP (Top View)



176-Pin TQFP

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V_{CCI}	V_{CCI}	V_{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V_{CCA}	V_{CCA}	V_{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V_{CCI}	V_{CCI}	V_{CCI}
33	V_{CCA}	V_{CCA}	V_{CCA}
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND

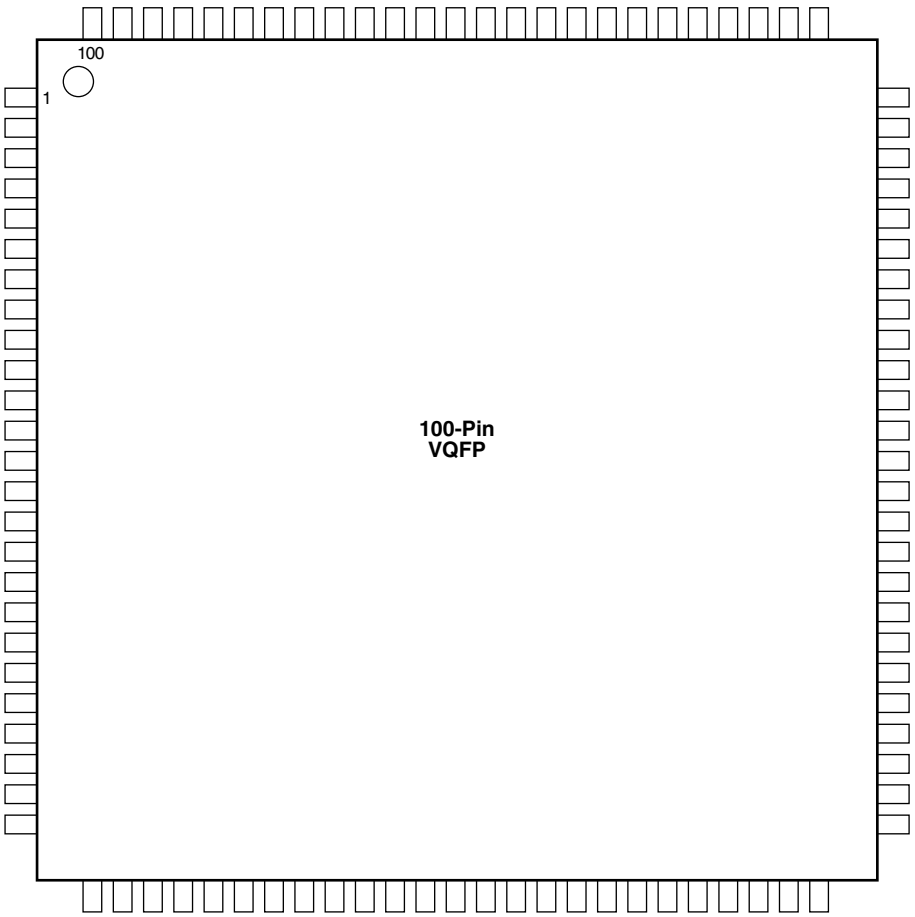
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V_{CCI}	V_{CCI}	V_{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V_{CCA}	V_{CCA}	V_{CCA}
67	V_{CCR}	V_{CCR}	V_{CCR}
68	I/O	I/O	I/O
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O

176-Pin TQFP (Continued)

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	V_{CCI}	V_{CCI}	V_{CCI}
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V_{CCA}	V_{CCA}	V_{CCA}
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V_{CCA}	V_{CCA}	V_{CCA}
123	GND	GND	GND
124	V_{CCI}	V_{CCI}	V_{CCI}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	I/O	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	CLKA	CLKA	CLKA
153	CLKB	CLKB	CLKB
154	V_{CCR}	V_{CCR}	V_{CCR}
155	GND	GND	GND
156	V_{CCA}	V_{CCA}	V_{CCA}
157	PRA, I/O	PRA, I/O	PRA, I/O
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	V_{CCI}	V_{CCI}	V_{CCI}
170	I/O	I/O	I/O
171	NC	I/O	I/O
172	NC	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

100-Pin VQFP (Top View)



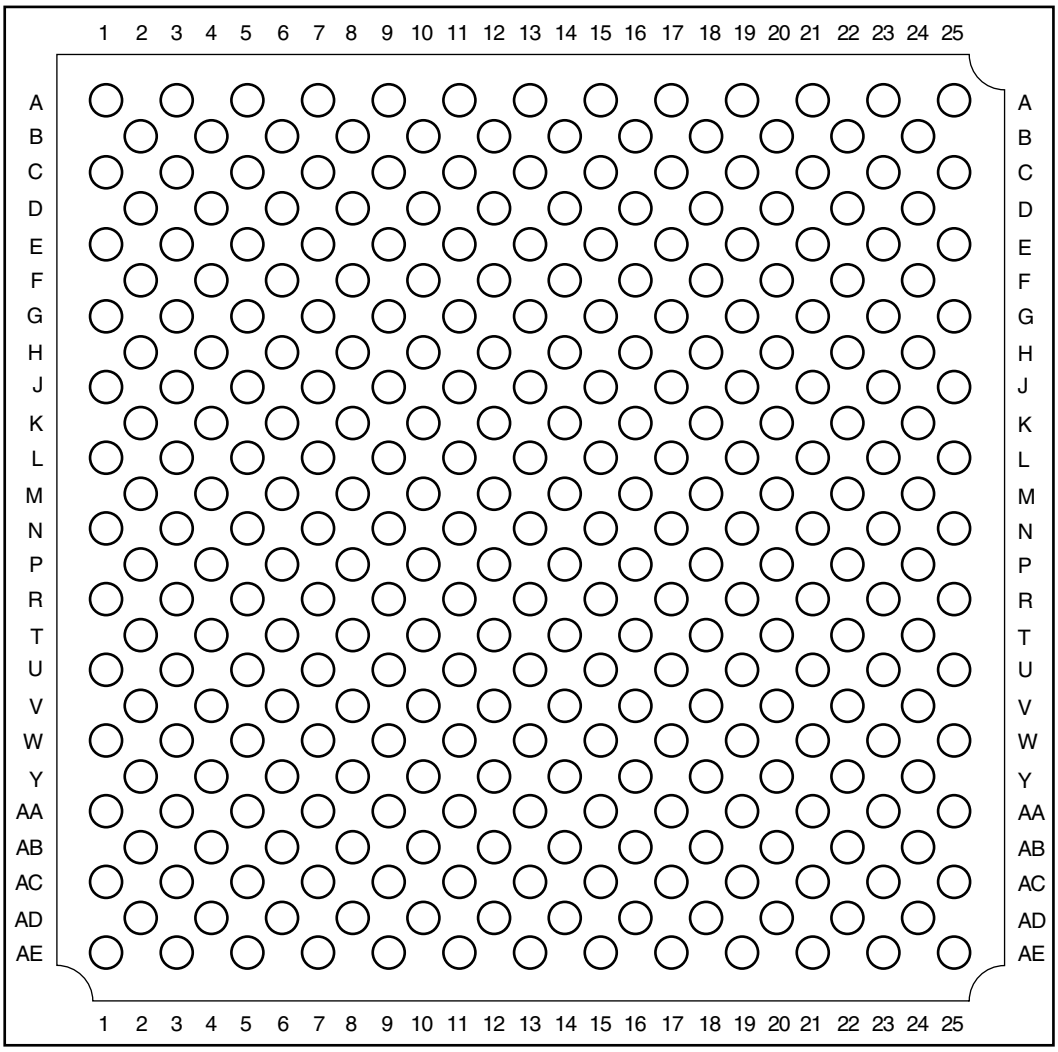
100-VQFP

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V_{CCI}	V_{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V_{CCI}	V_{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}
36	GND	GND
37	V_{CCR}	V_{CCR}
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V_{CCI}	V_{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O

Pin Number	A54SX08 Function	A54SX16 A54SX16P Function
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V_{CCA}	V_{CCA}
68	GND	GND
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V_{CCI}	V_{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V_{CCR}	V_{CCR}
90	V_{CCA}	V_{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

313-Pin PBGA (Top View)



313-Pin PBGA

Pin Number	A54SX32 Function
A1	GND
A3	NC
A5	I/O
A7	I/O
A9	I/O
A11	I/O
A13	V_{CCR}
A15	I/O
A17	I/O
A19	I/O
A21	I/O
A23	NC
A25	GND
AA1	I/O
AA3	I/O
AA5	NC
AA7	I/O
AA9	NC
AA11	I/O
AA13	I/O
AA15	I/O
AA17	I/O
AA19	I/O
AA21	I/O
AA23	NC
AA25	I/O
AB2	NC
AB4	NC
AB6	I/O
AB8	I/O
AB10	I/O
AB12	I/O
AB14	I/O
AB16	I/O
AB18	V_{CCI}
AB20	NC
AB22	I/O
AB24	I/O
AC1	I/O
AC3	I/O
AC5	I/O
AC7	I/O
AC9	I/O
AC11	I/O
AC13	V_{CCR}

Pin Number	A54SX32 Function
AC15	I/O
AC17	I/O
AC19	I/O
AC21	I/O
AC23	I/O
AC25	NC
AD2	GND
AD4	I/O
AD6	V_{CCI}
AD8	I/O
AD10	I/O
AD12	PRB, I/O
AD14	I/O
AD16	I/O
AD18	I/O
AD20	I/O
AD22	NC
AD24	I/O
AE1	NC
AE3	I/O
AE5	I/O
AE7	I/O
AE9	I/O
AE11	I/O
AE13	V_{CCA}
AE15	I/O
AE17	I/O
AE19	I/O
AE21	I/O
AE23	TDO, I/O
AE25	GND
B2	TCK, I/O
B4	I/O
B6	I/O
B8	I/O
B10	I/O
B12	I/O
B14	I/O
B16	I/O
B18	I/O
B20	I/O
B22	I/O
B24	I/O
C1	TDI, I/O
C3	I/O

Pin Number	A54SX32 Function
C5	NC
C7	I/O
C9	I/O
C11	I/O
C13	V_{CCI}
C15	I/O
C17	I/O
C19	V_{CCI}
C21	I/O
C23	I/O
C25	NC
D2	I/O
D4	NC
D6	I/O
D8	I/O
D10	I/O
D12	I/O
D14	I/O
D16	I/O
D18	I/O
D20	I/O
D22	I/O
D24	NC
E1	I/O
E3	NC
E5	I/O
E7	I/O
E9	I/O
E11	I/O
E13	V_{CCA}
E15	I/O
E17	I/O
E19	I/O
E21	I/O
E23	I/O
E25	I/O
F2	I/O
F4	I/O
F6	NC
F8	I/O
F10	NC
F12	I/O
F14	I/O
F16	NC
F18	I/O

Pin Number	A54SX32 Function
F20	I/O
F22	I/O
F24	I/O
G1	I/O
G3	TMS
G5	I/O
G7	I/O
G9	V_{CCI}
G11	I/O
G13	CLKB
G15	I/O
G17	I/O
G19	I/O
G21	I/O
G23	I/O
G25	I/O
H2	I/O
H4	I/O
H6	I/O
H8	I/O
H10	I/O
H12	PRA, I/O
H14	I/O
H16	I/O
H18	NC
H20	I/O
H22	V_{CCI}
H24	I/O
J1	I/O
J3	I/O
J5	I/O
J7	NC
J9	I/O
J11	I/O
J13	CLKA
J15	I/O
J17	I/O
J19	I/O
J21	GND
J23	I/O
J25	I/O
K2	I/O
K4	I/O
K6	I/O
K8	V_{CCI}

313-Pin PBGA (Continued)

Pin Number	A54SX32 Function
K10	I/O
K12	I/O
K14	I/O
K16	I/O
K18	I/O
K20	V_{CCA}
K22	I/O
K24	I/O
L1	I/O
L3	I/O
L5	I/O
L7	I/O
L9	I/O
L11	I/O
L13	GND
L15	I/O
L17	I/O
L19	I/O
L21	I/O
L23	I/O
L25	I/O
M2	I/O
M4	I/O
M6	I/O
M8	I/O
M10	I/O
M12	GND
M14	GND
M16	V_{CCI}
M18	I/O
M20	I/O
M22	I/O
M24	I/O
N1	I/O

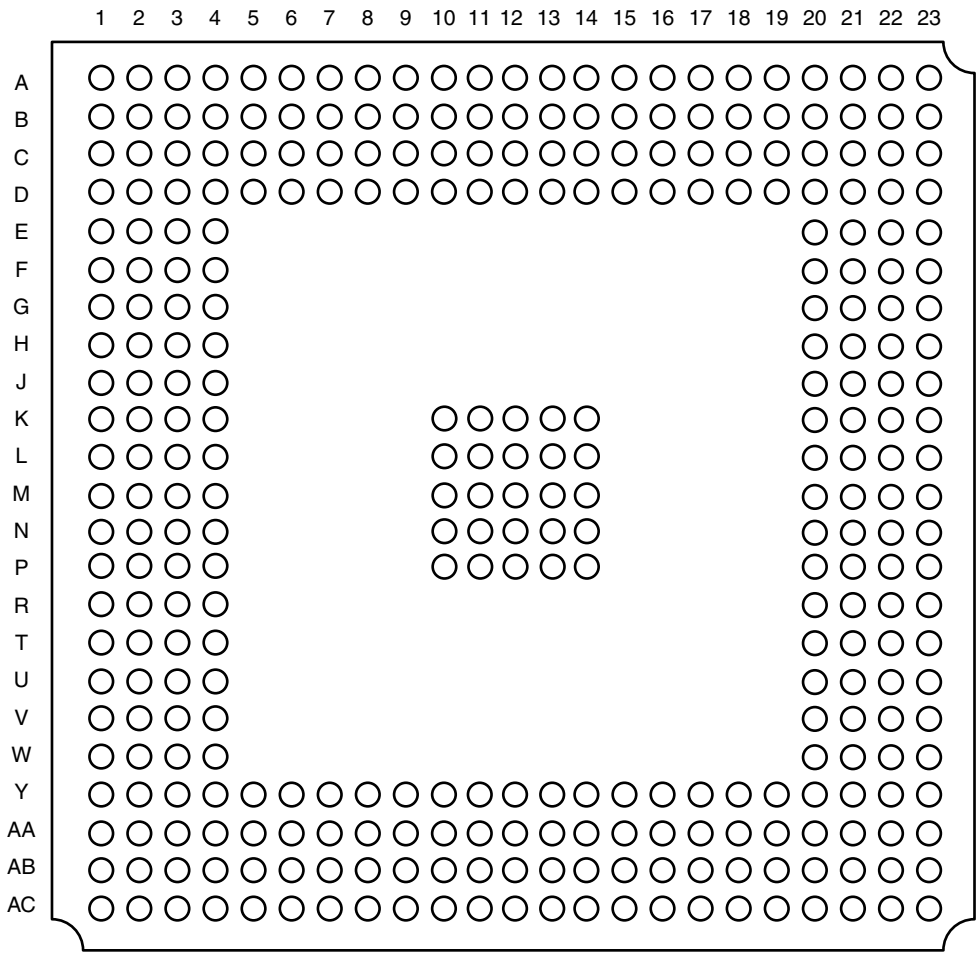
Pin Number	A54SX32 Function
N3	V_{CCA}
N5	V_{CCR}
N7	I/O
N9	V_{CCI}
N11	GND
N13	GND
N15	GND
N17	I/O
N19	I/O
N21	I/O
N23	V_{CCR}
N25	V_{CCA}
P2	I/O
P4	I/O
P6	I/O
P8	I/O
P10	I/O
P12	GND
P14	GND
P16	I/O
P18	I/O
P20	NC
P22	I/O
P24	I/O
R1	I/O
R3	I/O
R5	I/O
R7	I/O
R9	I/O
R11	I/O
R13	GND
R15	I/O
R17	I/O
R19	I/O

Pin Number	A54SX32 Function
R21	I/O
R23	I/O
R25	I/O
T2	I/O
T4	I/O
T6	I/O
T8	I/O
T10	I/O
T12	I/O
T14	HCLK
T16	I/O
T18	I/O
T20	I/O
T22	I/O
T24	I/O
U1	I/O
U3	I/O
U5	V_{CCI}
U7	I/O
U9	I/O
U15	I/O
U17	I/O
U19	I/O
U21	I/O
U23	I/O
U25	I/O
V2	V_{CCA}
V4	I/O
V6	I/O
V8	I/O
V10	I/O
V12	I/O
V14	I/O
V16	NC

Pin Number	A54SX32 Function
V18	I/O
V20	I/O
V22	V_{CCA}
V24	V_{CCI}
W1	I/O
W3	I/O
W5	I/O
W7	NC
W9	I/O
W11	I/O
W13	V_{CCI}
W15	I/O
W17	I/O
W19	I/O
W21	I/O
W23	I/O
W25	I/O
Y2	I/O
Y4	I/O
Y6	I/O
Y8	I/O
Y10	I/O
Y12	I/O
Y14	I/O
Y16	I/O
Y18	I/O
Y20	NC
Y22	I/O
Y24	NC

Package Pin Assignments (continued)

329-Pin PBGA (Top View)



329-Pin PBGA

Pin Number	A54SX32 Function
A1	GND
A2	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
AA1	V_{CCI}
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O

Pin Number	A54SX32 Function
AA23	V_{CCI}
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND
AC2	V_{CCI}
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V_{CCI}
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC

Pin Number	A54SX32 Function
AC22	V_{CCI}
AC23	GND
B1	V_{CCI}
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O

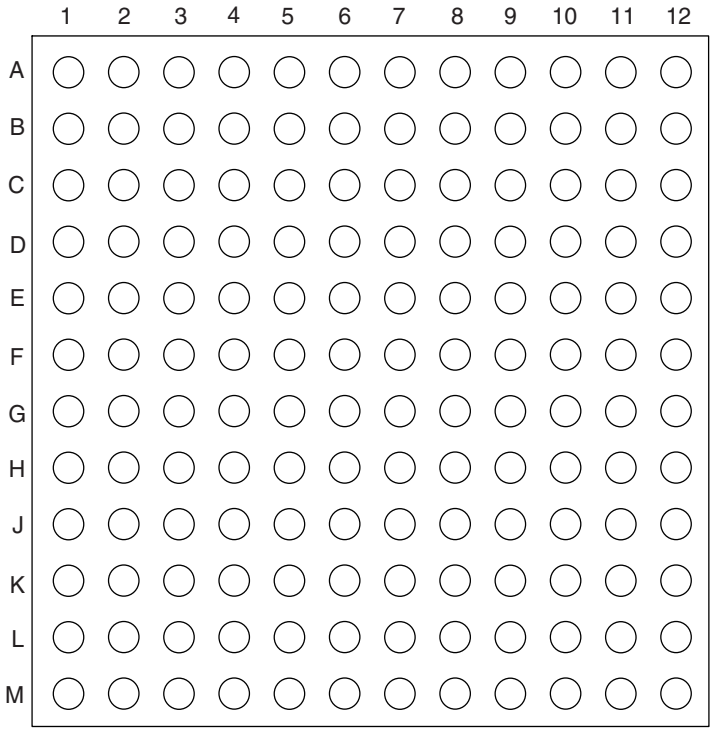
Pin Number	A54SX32 Function
C21	V_{CCI}
C22	GND
C23	NC
D1	I/O
D2	I/O
D3	I/O
D4	TCK, I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	V_{CCA}
D12	V_{CCR}
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
E1	V_{CCI}
E2	I/O
E3	I/O
E4	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
F1	I/O
F2	TMS
F3	I/O
F4	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
G1	I/O
G2	I/O
G3	I/O

329-Pin PBGA

Pin Number	A54SX32 Function
G4	I/O
G20	I/O
G21	I/O
G22	I/O
G23	GND
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H20	V_{CCA}
H21	I/O
H22	I/O
H23	I/O
J1	NC
J2	I/O
J3	I/O
J4	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K20	I/O
K21	I/O
K22	I/O
K23	I/O
L1	I/O
L2	I/O
L3	I/O
L4	V_{CCR}
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L20	V_{CCR}
L21	I/O
L22	I/O
L23	NC
M1	I/O
M2	I/O
M3	I/O
M4	V_{CCA}
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M20	V_{CCA}
M21	I/O
M22	I/O
M23	V_{CCI}
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N20	NC
N21	I/O
N22	I/O
N23	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P20	I/O
P21	I/O
P22	I/O
P23	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R20	I/O
R21	I/O
R22	I/O
R23	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T20	I/O
T21	I/O
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V_{CCA}
U4	I/O
U20	I/O
U21	V_{CCA}
U22	I/O
U23	I/O
V1	V_{CCI}
V2	I/O
V3	I/O
V4	I/O
V20	I/O
V21	I/O
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V_{CCA}
Y13	V_{CCR}
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

Package Pin Assignments (Continued)

144-Pin FBGA (Top View)



144-Pin FBGA

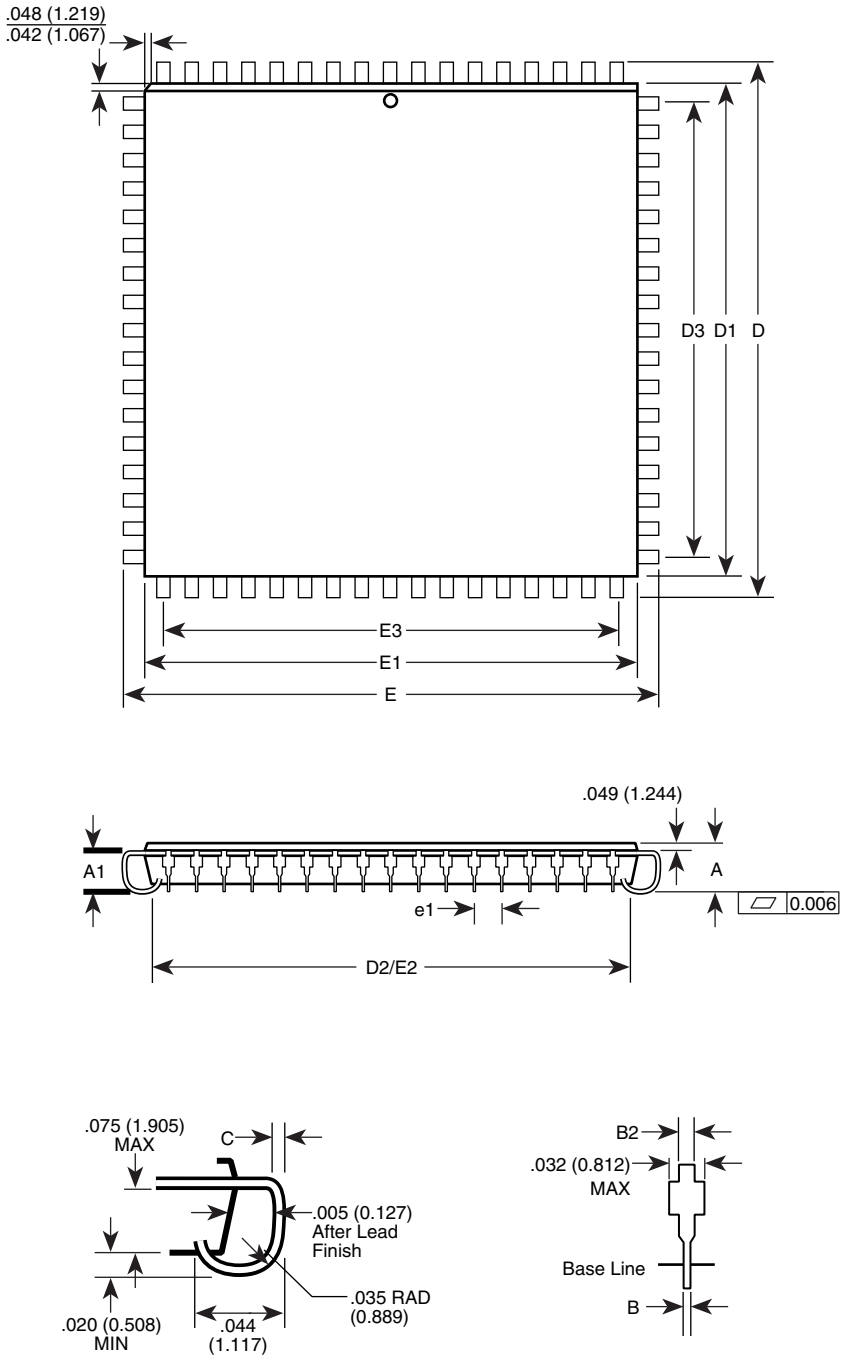
Pin Number	A54SX08 Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	V_{CCA}
A6	GND
A7	CLKA
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
B1	I/O
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	CLKB
B8	I/O
B9	I/O
B10	I/O
B11	GND
B12	I/O
C1	I/O
C2	I/O
C3	TCK, I/O
C4	I/O
C5	I/O
C6	PRA, I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
D1	I/O
D2	V_{CCI}
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O

Pin Number	A54SX08 Function
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	TMS
E6	V_{CCI}
E7	V_{CCI}
E8	V_{CCI}
E9	V_{CCA}
E10	I/O
E11	GND
E12	I/O
F1	I/O
F2	I/O
F3	V_{CCR}
F4	I/O
F5	GND
F6	GND
F7	GND
F8	V_{CCI}
F9	I/O
F10	GND
F11	I/O
F12	I/O
G1	I/O
G2	GND
G3	I/O
G4	I/O
G5	GND
G6	GND
G7	GND
G8	V_{CCI}
G9	I/O
G10	I/O
G11	I/O
G12	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	V_{CCA}
H6	V_{CCA}
H7	V_{CCI}
H8	V_{CCI}
H9	V_{CCA}
H10	I/O
H11	I/O
H12	V_{CCR}

Pin Number	A54SX08 Function
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J6	PRB, I/O
J7	I/O
J8	I/O
J9	I/O
J10	I/O
J11	I/O
J12	V_{CCA}
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	GND
K8	I/O
K9	I/O
K10	GND
K11	I/O
K12	I/O
L1	GND
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	HCLK
L8	I/O
L9	I/O
L10	I/O
L11	I/O
L12	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	V_{CCA}
M8	I/O
M9	I/O
M10	I/O
M11	TDO, I/O
M12	I/O

Package Mechanical Drawings

Plastic Leaded Chip Carrier (PLCC)



Plastic Leaded Chip Carrier Packages (PLCC)

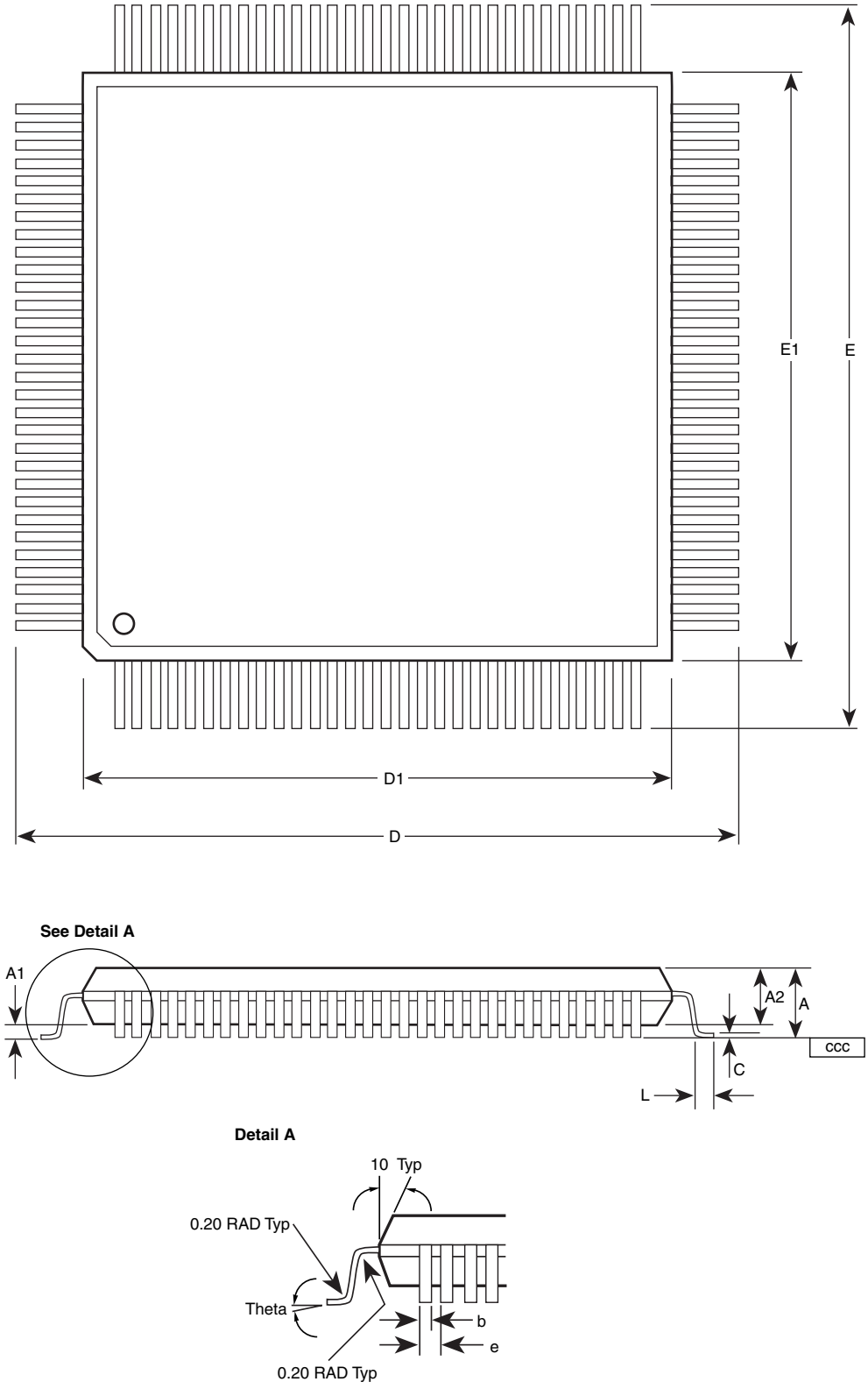
JEDEC Equiv	PLCC 84 MS007 AE VAR	
Dimension	**Min.**	**Max**
A	3.94	4.45
A1	2.29	3.30
B	0.33	0.69
B2	0.66	0.81
C	0.13	0.28
D/E	29.72	30.73
D1/E1	28.96	29.46
D2/E2	27.69	28.70
D3/E3	25.4 nominal	
e1	1.27 BSC	

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

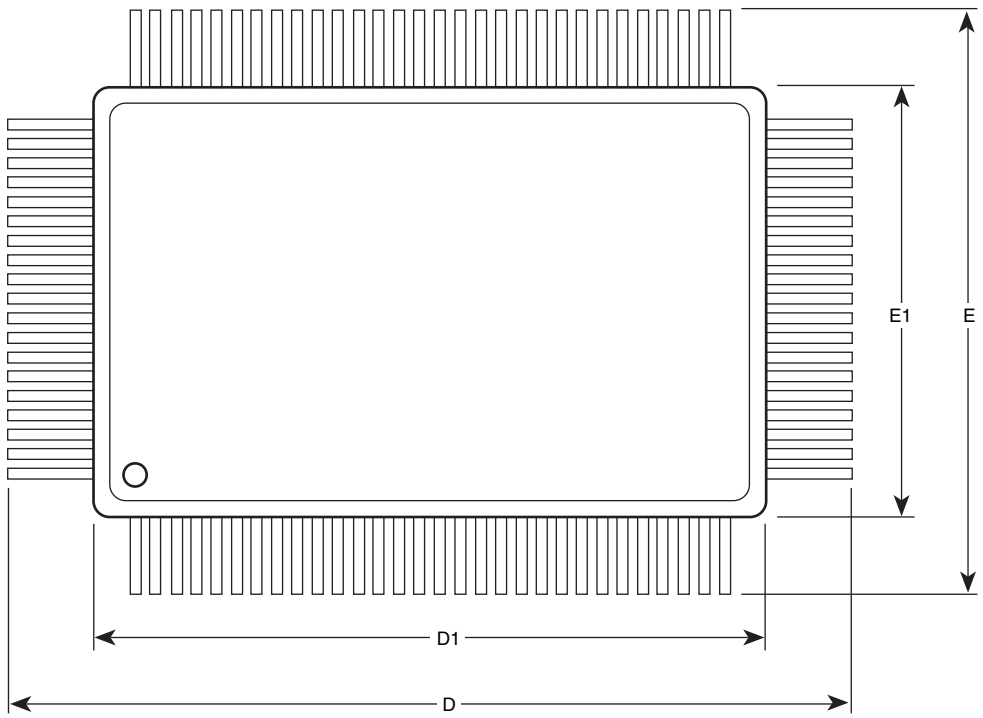
Package Mechanical Drawings (continued)

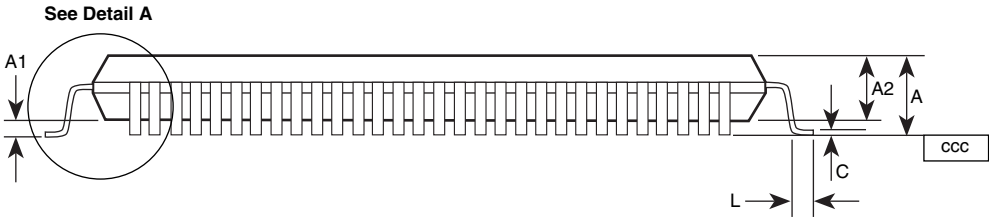
Plastic Quad Flat Pack (PQFP, TQFP, VQFP)

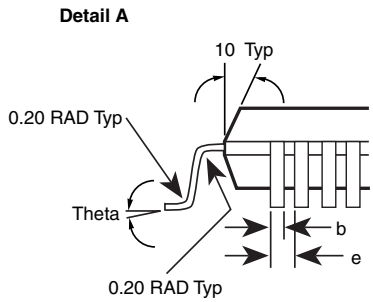


Package Mechanical Drawings (continued)

Plastic Quad Flat Pack
Rectangular Package (PQFP)







Plastic Quad Flat Packs (PQFP)

JEDEC Equiv	PQFP 208 MO-143		
Dimension	**Min.**	**Nom**	**Max**
A		3.70	4.10
A1	0.25	0.38	
A2	3.20	3.40	3.60
b	0.17		0.27
c	0.09		0.20
D/E	30.25	30.60	30.85
D1/E1	27.90	28.00	28.10
e	0.50 BSC		
L	0.50	0.60	0.75
ccc			0.10
Theta	0		7 deg
Diameter	19.82	20.32	20.82

Thin Quad Flat Packs (TQFP)

JEDEC Equiv	TQFP 144 MO-136			TQFP 176 MO-136		
Dimension	**Min.**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A			1.60			1.60
A1	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
b	0.17		0.27	0.17		0.27
c	0.09		0.20	0.09		0.20
D/E	21.75	22.00	22.25	25.75	26.00	26.25
D1/E1	19.90	20.00	20.10	23.90	24.00	24.10
e	0.50 BSC			0.50 BSC		
L	0.45	0.60	0.75	0.45	0.60	0.75
ccc			0.10			0.10
Theta	0		7 deg	0		7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Thin Quad Flat Packs (VQFP)

JEDEC Equiv	VQFP 100 MO-136		
Dimension	**Min**	**Nom**	**Max**
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17		0.27
c	0.09		0.20
D/E	15.75	16.00	16.25
D1/E1	13.90	14.00	14.10
e		0.50 BSC	
L	0.45	0.60	0.75
ccc			0.10
Theta	0		7 deg

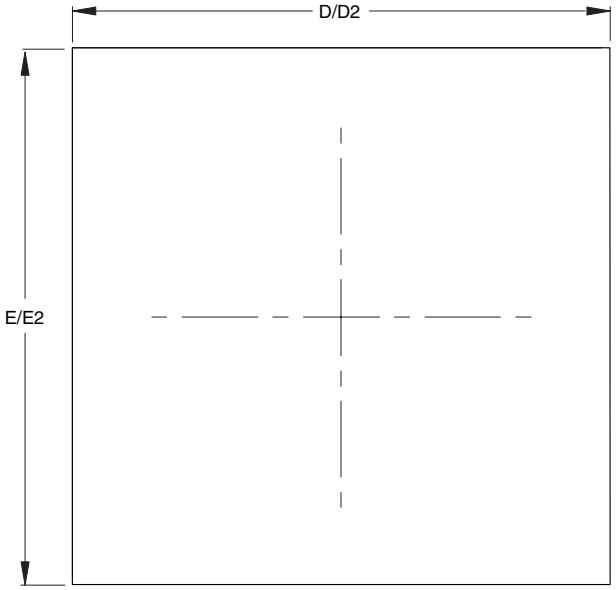
Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

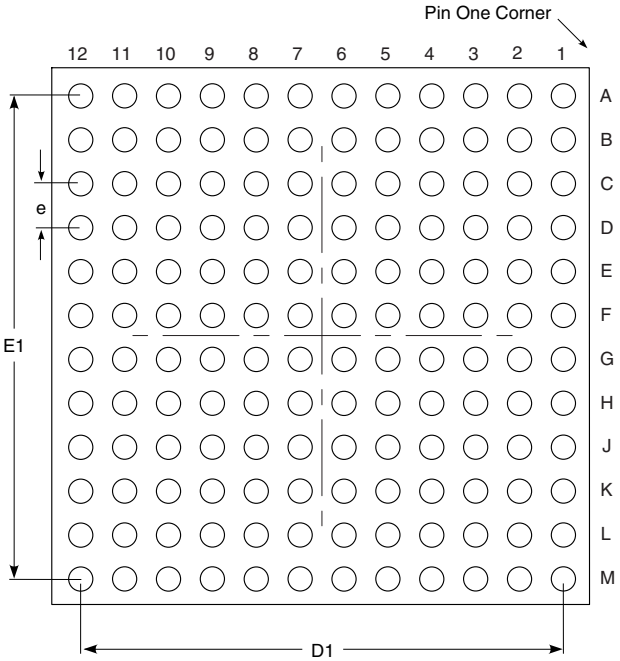
Package Mechanical Drawings (continued)

144-Pin FBGA

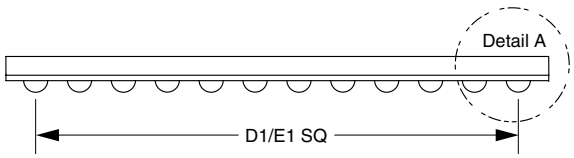
Top View



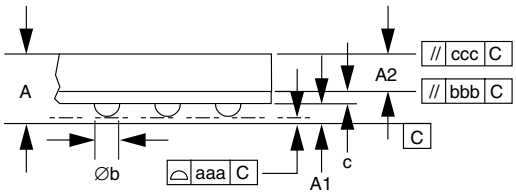
Bottom View



Side View



Detail A



Fine Pitch Ball Grid Array (FBGA)

	FBGA 144		
Dimension	**Min.**	**Nom.**	**Max.**
A	1.35	1.45	1.55
A1	0.35	0.40	0.45
A2	0.65	0.70	0.75
aaa			0.15
b	0.45	0.50	0.55
bbb			0.20
c		0.35	
ccc			0.25
D	12.80	13.00	13.20
D1		11.00 BSC	
D2	12.80	13.00	13.20
E	12.80	13.00	13.20
E1		11.00 BSC	
E2	12.80	13.00	13.20
e	0.9	1.00	1.10

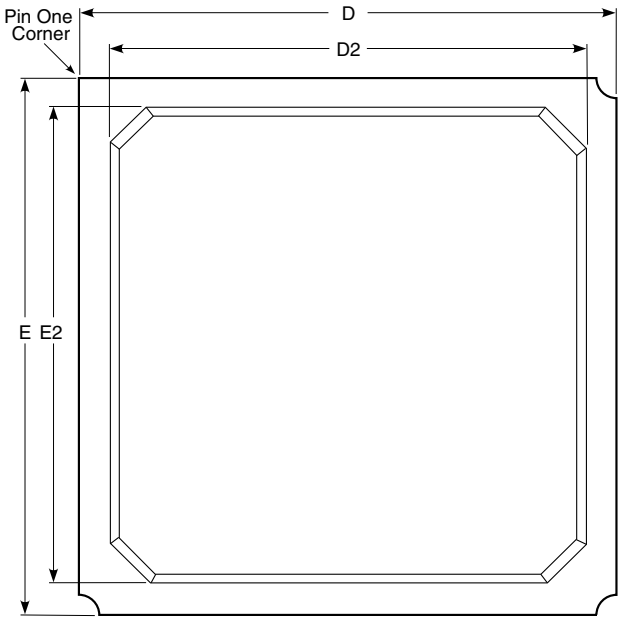
Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

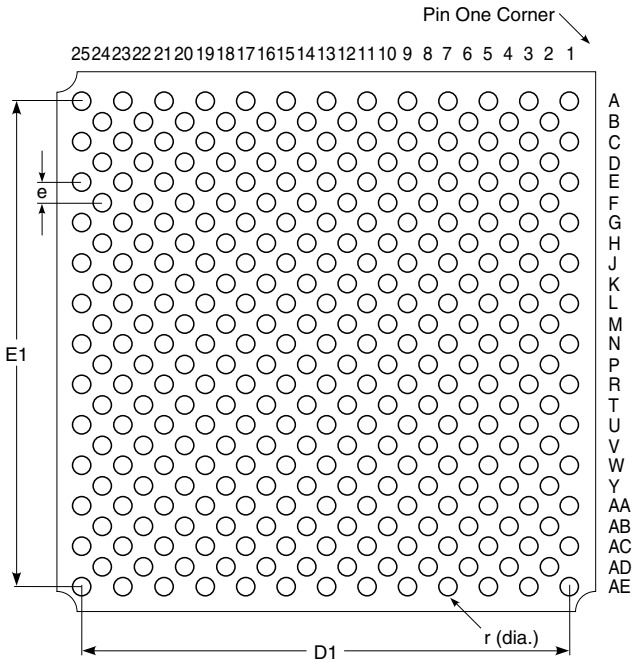
Package Mechanical Drawings (continued)

Plastic Ball Grid Array (PBGA313)

Top View

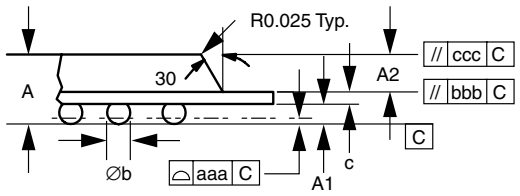


Bottom View



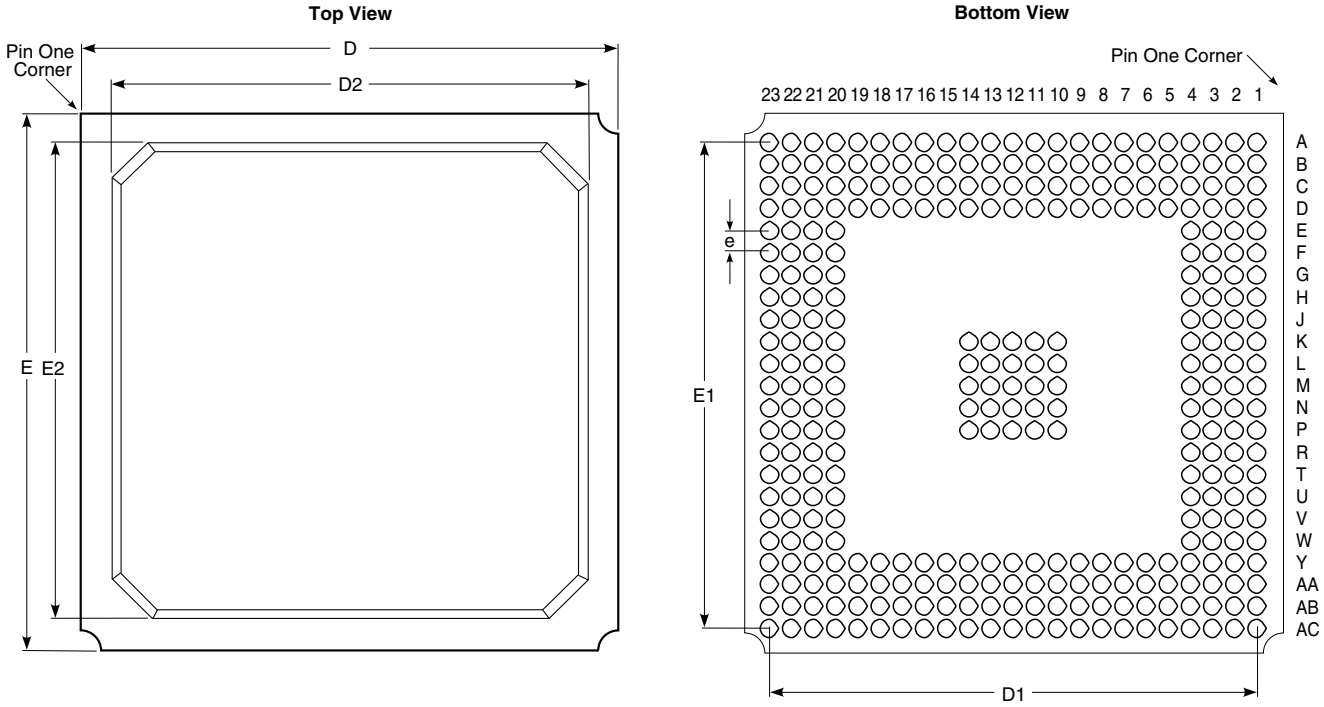
Side View

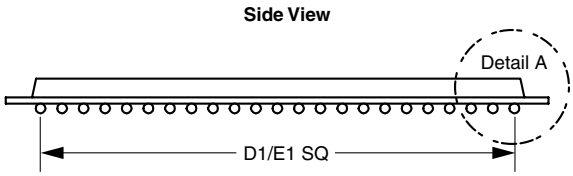
Detail A

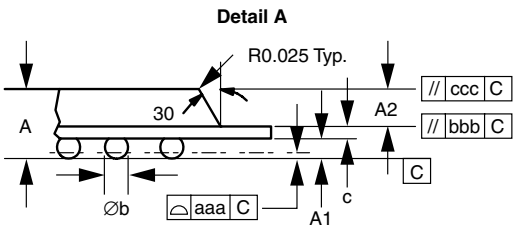


Package Mechanical Drawings (continued)

Plastic Ball Grid Array (PBGA329)







Plastic Ball Grid Array (PBGA)

JEDEC Equivalent	PBGA313			PBGA329		
Dimension	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	2.12	2.33	2.52	2.17	2.33	2.70
A1	0.50	0.60	0.70	0.50	0.60	0.70
A2	1.12	1.17	1.22	1.10	1.20	1.30
D	34.80	35.00	35.20	30.80	31.00	31.20
D1		30.48 BSC			27.94 BSC	
D2	29.50	30.00	30.70	27.90	28.00	28.10
E	34.80	35.00	35.20	30.80	31.00	31.20
E1		30.48 BSC			27.94 BSC	
E2	29.50	30.00	30.70	27.90	28.00	28.10
b	0.60	0.76	0.90	0.60	0.76	0.90
c	0.53	0.56	0.61	0.53	0.60	0.70
aaa			0.15			0.20
bbb			N/A			0.20
ccc			0.35			0.25
e		1.27 typ.			1.27 typ.	

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

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