Silicon Expert

User's Guide

Actel

Windows® and UNIX® Environments

Actel Corporation, Sunnyvale, CA 94086

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Introduction

The *Silicon Expert User's Guide* contains detailed information about using the Silicon Expert tool of the Designer Series software.

Silicon Expert reads in a netlist (.edn) file, and allows you to optimize designs for Actel devices, translate designs into various EDIF flavors, print out a timing report of your optimized design, and write an optimized structural netlist for place and route with Actel's Designer.

Also included in this guide is a tour that describes usage examples of Silicon Expert. Refer to the *Designing with Actel* manual for additional information about using the Designer software.

Document Organization

The *Silicon Expert User's Guide* is divided into the following chapters:

Chapter 1 - Design Flow contains information describing how Silicon Expert integrates into a schematic-based or a synthesis-based design flow.

Chapter 2- I/O Macro Manager gives detailed information about the I/O Macro Manager feature of Silicon Expert.

Chapter 3-Buffer Manager gives detailed information about the Buffer Manager feature of Silicon Expert.

Chapter 4- Translate gives detailed information about the Translate feature of Silicon Expert.

Chapter 5- Design Report gives detailed information about the Design Report feature of Silicon Expert.

Chapter 6- Touring Silicon Expert gives examples of using Silicon Expert.

Appendix A - Menus, Commands, and Shortcut Toolbar gives detailed information about the menus, commands, and the shortcut toolbar used in Silicon Expert

Appendix B - Read Netlist Dialog Box gives detailed information about the Read Netlist dialog box of Silicon Expert

Appendix C - Write Netlist Dialog Box - gives detailed information about the Write Netlist dialog box of Silicon Expert

Appendix D - Product Support - Provides information about contacing Actel for customer and technical support

Document Assumptions

The information in this manual is based on the following assumptions:

1. You have installed the Designer Series software and the Silicon Expert tool. If you need to install Designer Series software and Silicon Expert, refer to the installation instructions in the *Designing with Actel* manual.
2. You are familiar with UNIX workstations and UNIX operating systems, or with PCs and Windows operating environments.
3. You are familiar with FPGA architecture and FPGA design software.

This manual uses screens from the PC version of Silicon Expert. UNIX screens appear slightly different, but the functionality is the same.

Actel Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the on-line manuals, you must install Adobe® Acrobat Reader® from the CD-Rom.

The Designer Series includes the following manuals, which provide additional information about designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

DeskTOP Interface Guide. This guide contains information about using the integrated VeriBest® and Synplicity® CAE software tools with the Actel Designer Series FPGA development tools to create designs for Actel Devices.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic Powerview® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

Actel FPGA Data Book. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

Context Sensitive On-Line Help

Silicon Expert features context sensitive on-line help. Context-sensitive on-line help lets you point to any item on the screen and get specific information about that item.

To use context sensitive on-line help, do one of the following:

- (PC only) Choose the Help button on the toolbar, place the cursor over the item on the screen you need help with, and then click the left mouse button. An informational pop-up topic will appear.
- (PC only) Place the cursor over the item on the screen you need help with, and press the F1 function key. An informational pop-up topic will appear.
- Place the cursor over the item on the screen you need help with, and click the right mouse button. This displays the “What’s This” pop up. Click the left mouse button. An informational pop-up topic will appear.

1

Design Flow

This chapter contains information about how Silicon Expert fits into a typical Actel schematic- or synthesis-based design flow. Also contained in this chapter is an overview of Silicon Expert.

Schematic- or Synthesis-Based Design Flow

The Actel schematic- or synthesis-based design flow has four main steps; Design Creation/Verification, Design Implementation, Programming, and System Verification. A typical design flow using Silicon Expert is shown in Figure 1-1.[1]

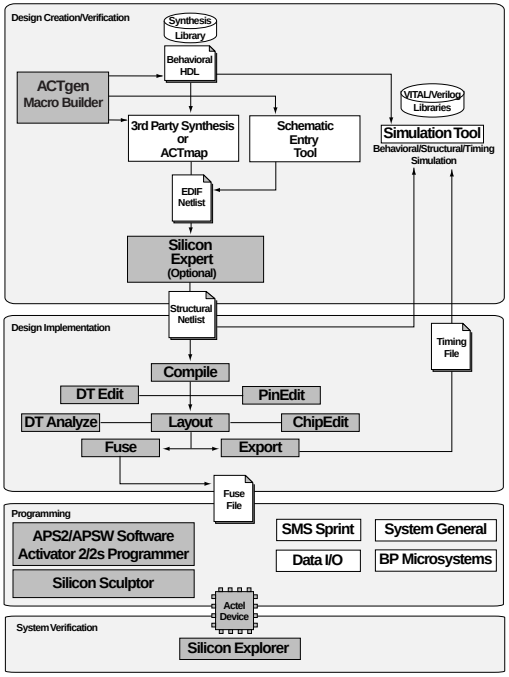

Figure 1-1. Silicon Expert Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 1-1.

Silicon Expert can be used during design creation to add I/Os to a design or balance buffer trees. Silicon Expert can also be used after design creation to translate a structural netlist from one format to another. For more detailed information about typical Actel synthesis- and schematic-based design flows, refer to the *Designing With Actel* manual.

Overview of Silicon Expert

This section provides an overview of the Silicon Expert tool. More detailed information can be found in the chapters "I/O Macro Manager" on page 5, "Translate" on page 13, "Design Report" on page 15, "Touring Silicon Expert" on page 21, and "Menus, Commands, and Shortcut Toolbar" on page 39.

Silicon Expert reads in a netlist (.edn) file, and allows you to optimize designs for Actel devices, translate designs into various EDIF flavors, print out a timing report of your optimized design, and write an optimized structural netlist for place and route with Actel's Designer.

Invoking Silicon Expert

Perform the following steps to invoke Silicon Expert on a PC or UNIX workstation.

PC

From the Windows Start bar, click Programs, click Designer R1-1999, and then click the Silicon Expert icon in the Designer R1-1999 program group.

UNIX

From the command line, type the following:

```
expert
```

This will invoke the Silicon Expert window. The Silicon Expert window displays log and timing report information about the netlist. The Silicon Expert window is shown in Figure 1-2.

Refer to “Viewing a Report” on page 18 for information about Timing Reports displayed in the Silicon Expert window.

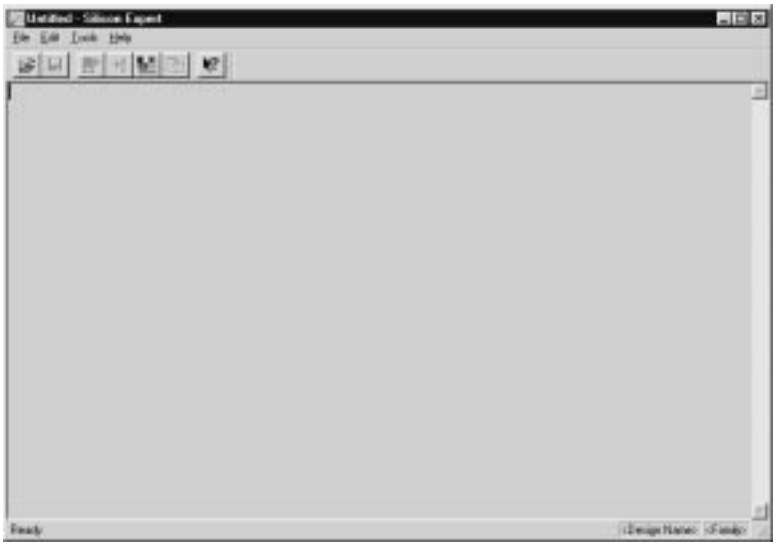

Figure 1-2. Silicon Expert Window

When you invoke Silicon Expert program, the Silicon Expert Window is diplayed. From this window, you can observe the progress of design optimization, and read reports.

You can clear the information displayed on Silicon Expert window by clicking the clear command in the Edit menu.

Following are descriptions of I/O Macro Manager, Buffer Manager, Translate, and Design Report features of Silicon Expert.

I/O Macro Manager

I/O Macro Manager allows you to perform the following tasks to optimize your Actel designs:

- Insert, replace, or correct pads
- Insert global clocks on selected networks

For more detailed information about the I/O Macro Manager refer to "I/O Macro Manager" on page 5.

Buffer Manager

Buffer Manager allows you to:

- Buffer high fanout nets and rebuffer networks
- Insert internally driven global clocks on selected networks

For more detailed information about the Buffer Manager refer to "Buffer Manager" on page 9.

Translate

Translate allows you to translate a structural netlist from a given format into a different format.

The Translate function can read EDIF, Verilog, and ADL netlists, and translate them into EDIF, Verilog, VHDL, or ADL netlist formats. For more detailed information about Translate, refer to "Translate" on page 13.

Design Report

Design Report generates a report with the following information:

- Utilization of chip resources, such as number of sequential and logic modules
- Worst/longest estimated timing paths in the design

For more detailed information about Design Report, refer to "Design Report" on page 15.

2

I/O Macro Manager

This chapter describes the features of the Silicon Expert I/O Macro Manager. I/O Macro Manager enables you to take full advantage of architecture-specific features of Actel devices. Using the I/O Macro Manager, you can perform pad/registered pad insertion for designs with no pads or pads inserted on only a portion of the design, incorporate expertise within the system to carry out all operations autonomously and utilize global resources such as Clkbuf and Hclkbuf.

Using I/O Macro Manager

You can invoke I/O Macro Manager two ways:

1. **Select I/O Macro Manager from the Tools menu.** Refer to "Menus, Commands, and Shortcut Toolbar" on page 39 for information about how to use the Tools menu.
2. **Select the I/O Macro Manager from the Shortcut Toolbar.** Refer to "Silicon Expert Shortcut Toolbar" on page 42 for information about how to use the Shortcut Toolbar.

Read a Netlist

When Silicon Expert is invoked, if a netlist has not yet been read in, you must click the **File** Menu and select the netlist you wish optimize from the "Read Netlist dialog box" before you can use the I/O Macro Manager. Refer to "Read Netlist Dialog Box" on page 45 for information about the Read Netlist dialog box.

Description of I/O Macro Manager Features

When I/O Macro Manager is invoked, a dialog box is displayed, as shown in Figure 2-1.

The I/O Macro Manager dialog box can also be displayed by selecting the I/O Macro Manager command in the Tools menu. Refer to "Tools Menu" on page 40 for more information about the Tools menu.

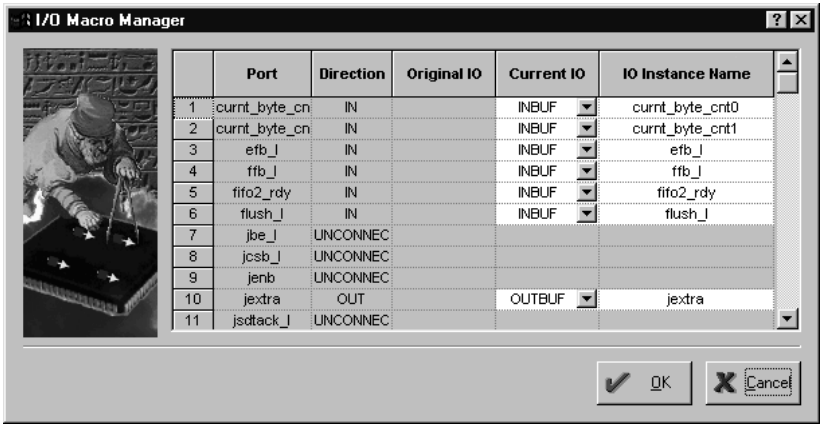

Figure 2-1. I/O Macro Manager dialog box

I/O Macro Manager Dialog Box

This section describes in detail the features of the I/O Macro Manager dialog box (Figure 2-1).

The I/O Macro Manager dialog box consists of the following spreadsheet columns and buttons:

Port Column

The Port column lists by name all of the ports found in the design.

Direction Column

The Direction column lists the port direction. If the port does not drive any cells, the word "UNCONNECTED" is displayed.

Original I/O Column

The Original I/O column displays the I/O Macro if it has already been inserted on the port. A blank indicates that an I/O Macro does not exist on the port.

Current I/O Column

The Current I/O column displays the best I/O macro for the given port, as suggested by Silicon Expert.

I/O Instance Name Column

The I/O Instance Name column displays the name of the I/O Macro.

OK Button

Click the OK button to finish the design with all actions performed up to this point.

Cancel Button

Click the Cancel button to cancel changes to your design.

3

Buffer Manager

This chapter describes the features of the Silicon Expert Buffer Manager. Like the I/O Manager, Buffer Manager enables you to take full advantage architecture specific features of Actel devices. Using the Buffer Manger you can balance, replace or correct buffer trees, insert buffer trees for high fanout nets, utilize global resources such as CLKINT, QCLKINT, for reset/preset networks or high fanout nets and perform complex netlist enhancement tasks.

Using Buffer Manager

You can invoke the Buffer Manager two ways:

1. **Select the Buffer Manager command in the Tools menu.** Refer to "Tools Menu" on page 40 for more information about the Tools menu.
2. **Select the Buffer Manageer from the Shortcut Toolbar.** Refer to "Silicon Expert Shortcut Toolbar" on page 42 for information about how to use the Shortcut Toolbar.

Description of Buffer Manager Features

When you invoke the Buffer Manager, a dialog box is displayed, as show in Figure 3-1. This section describes the features of the Buffer Manager dialog box.

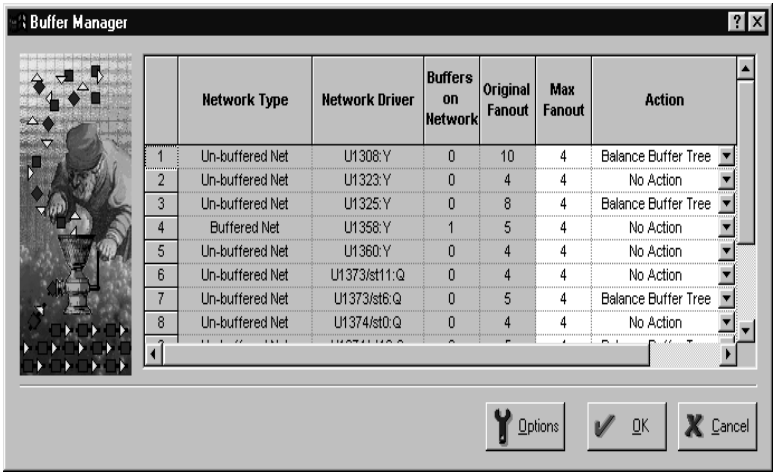

Figure 3-1. Buffer Manager dialog box

The Buffer Manager dialog box consists of the following spreadsheet columns and buttons:

Network Type Column

The Network Type column lists the type of the network.

Network Driver Column

The Network Driver column lists the hierarchical pin name of the driver of the network.

Buffers on Network Column

The Buffers on Network column lists the total number of buffers on the network.

Original Fanout Column

The Original Fanout column lists the total number of pins driven by the network. The buffers on the network are ignored.

Max Fanout Column

The Max Fanout column lists the maximum fanout for buffer tree creation.

Action Column

The Action column lists the action command to the Silicon Expert. The user can select the type of action that can be applied for the network.

OK Button

Click the OK button to finish the design with all actions performed up to this point.

Cancel Button

Click the Cancel button to cancel all actions performed on the design.

Buffer Manager Options

You can assign various optional constraints to your design in the Buffer Manager by using the The Buffer Manager Options. The Buffer Manager Options dialog box, shown in Figure 3-2, is displayed when you click the Options button on the Buffer Manager spreadsheet.

This section describes in detail the features of the Buffer Manager Options dialog box.

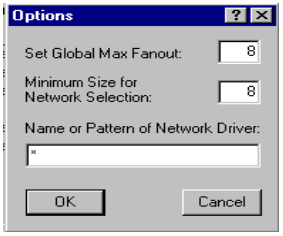

Figure 3-2. Buffer Manager Options Dialog box

Set Global Max Fanout Box

In the Global Max Fanout box, you can globally set the maximum fanout for all networks on the Max Fanout column of the Macro Manager spreadsheet.

Minimize Size for Network Selection Box

The Minimum Size for Network Selection box displays all the networks with a size above or equal to the given value.

Name or Pattern of Network Driver Box

The Name or Pattern of Network Driver box displays all the networks with a name matching the name you enter.

Write Netlist

When you have finished with the I/O Macro Manager spreadsheet, the Buffer Manager spreadsheet, and have clicked the OK button, the Write Netlist dialog box is displayed.

Name your netlist, select an output format, and save it. Refer to “Write Netlist Dialog Box” on page 49 for information about the Write Netlist dialog box.

4

Translate

The Translate function of Silicon Explorer performs the following functions: Reads netlist in EDIF, ADL, Verilog formats and writes it out as a netlist in EDIF, Verilog, ADL, or VHDL format, provides the user the ability to convert a netlist in one format to another and enables the user to select the different netlist input and output flavors.

Using Translate

You can invoke Translate two ways:

1. **Select Translate from the Tools menu.** Refer to "Menus, Commands, and Shortcut Toolbar" on page 39 for information about how to use the Tools menu.
2. **Invoke Translate from the Toolbar.** Refer to "Silicon Expert Shortcut Toolbar" on page 42 for information about how to use the Translate Wizard.

Read Netlist

When Translate is invoked, if a Netlist has not yet been read the Read Netlist dialog box is displayed. Select the netlist you wish to translate, and open it. Refer to "Read Netlist Dialog Box" on page 45 for information about the Read Netlist dialog box.

Write a Netlist

After your design is read in, the Write a Netlist dialog box is displayed. Name your netlist, select the output format, and save it. Refer to "Write Netlist Dialog Box" on page 49 for information about the Write a Netlist dialog box.

5

Design Report

Design Report performs the following: Reports area and timing numbers for a compiled Actel design or an Actel sub-design block, and provides user control of most of the compile options.

Using Design Report

You can invoke Design Report two ways:

1. **Select Design Report from the Tools menu.** Refer to "Menus, Commands, and Shortcut Toolbar" on page 39 for information about how to use the Tools menu.
2. **Invoke Design Report from the Toolbar.** Refer to "Silicon Expert Shortcut Toolbar" on page 42 for information about how to use the toolbar.

Read a Netlist

A netlist must be read into Silicon Expert before Design Report is invoked.To open a netlist, select the netlist you wish to optimize, and open it. Refer to "Read Netlist Dialog Box" on page 45 for information aboutdialog box the Read Netlist dialog box.

Design Report Variables Dialog Box

When a netlist is read, the Design Report Variables dialog box is displayed, as shown in Figure 5-1.

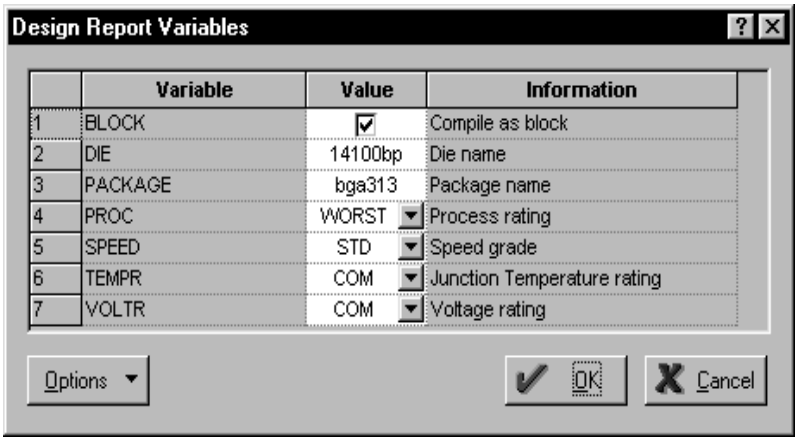

Figure 5-1. Design Report Variables dialog box

The Design Report dialog box consists of the following spreadsheet columns and buttons:

Variable Column

The Variable column displays the variable that controls the Report Generator.

Value Column

The Value column displays the value that can be applied to the variable. You can click check boxes, select commands from drop down menus, or fill in blanks, as needed, to modify displayed value.

Information Column

The Information column displays a brief description of the variable and its function.

Design Report Options

The Design Report Options dialog box is displayed when you click the Options button, located at the lower left of the Read a Netlist dialog box (Figure 5-1.). The following are descriptions of the Design Report options.

Apply Defaults

When you click the Apply Default option, the values in the Netlist Options spreadsheet are reset to the default values.

Advanced

When you click the Advanced option, additional netlister variables are displayed that allow advanced users more control over the netlister read operation.

Add Variables

When you click the Add Variables option, you can add undocumented netlister variables.

Viewing a Report

After setting all variables in the Design Report Variables dialog box, click OK to generate a report. A sample report is shown in Figure 5-2.

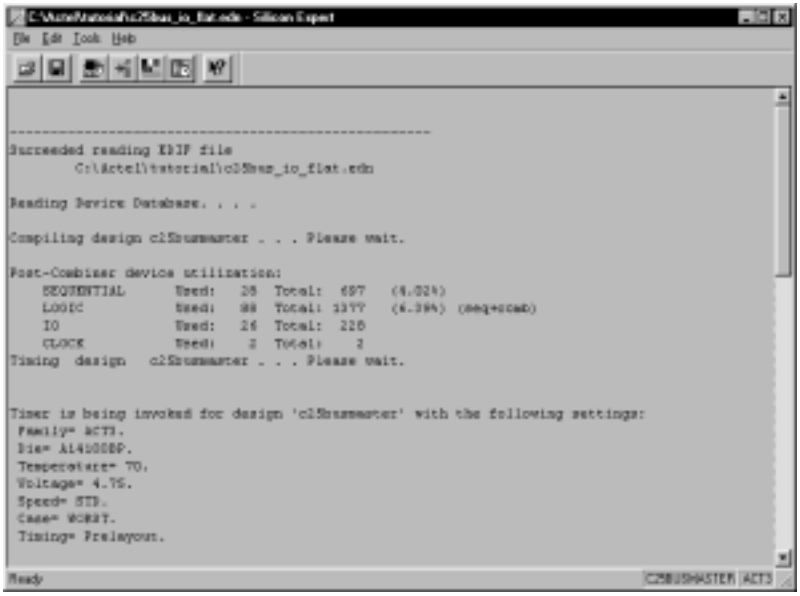

Figure 5-2. Sample Report

A report generated by Silicon Expert Design Report consists of an Area report section and Timing Report section.

Area Report

The Area report gives the count of sequential and combinatorial modules used by the design. The Area report also lists the number of I/O resources, clock resources, or special resources used in the design.

Timing Report

The pre-layout estimated timing is displayed for the following path groups:

- Port to Port
- Port to Register
- Register to Port
- Register to Register

6

Touring Silicon Expert

This chapter gives usage examples for using Silicon Expert to modify a design. Included are steps to read a sample netlist into Silicon Expert, compile the netlist as a block, set I/O buffers with the I/O Macro Manager, save the new netlist, run a design report, use the Buffer Manager options, observe the changes made by Buffer Manager, flatten a netlist, use Buffer Manager to change fanout of a design, and save a log file of your session.

Reading a Netlist to Generate a Report

This section describes how to read a netlist into Silicon Expert, and how to use the options available in the Read Netlist dialog box.

To read your design into Silicon Expert:

1. Invoke Silicon Expert.

PC

From the Windows Start bar, click Programs, click Designer R1-1999, and click the Silicon Expert icon in the Designer R1-1999 program group.

UNIX

From the command line, type the following:

```
expert
```

The Silicon Expert window is shown in Figure 6-1..

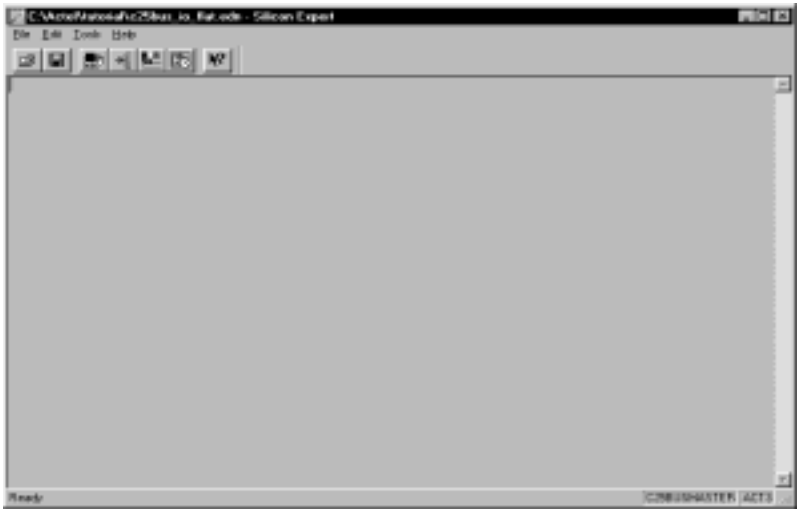

Figure 6-1. Silicon Expert Window

2. **Select the Read a Netlist command from the File menu.** This invokes the Read Netlist dialog box, as shown in Figure 6-2.

Figure 6-2. Read Netlist dialog box

3. **Select Edif Netlist (*.ed*) in the Files of Type pull down menu, as shown in Figure 6-2.**
4. **Select ACT 3 in the Family pull-down.**
5. **In the Look In box, navigate to the $ALSDIR/Tutorial directory, and select the file c25busmaster.edn.** This file is a EDIF file created specifically for this tour.
6. **Click the Options button at the lower right corner of the Read Netlist dialog box.** This displays the Read Netlist Options dialog box, as shown in Figure 6-3.

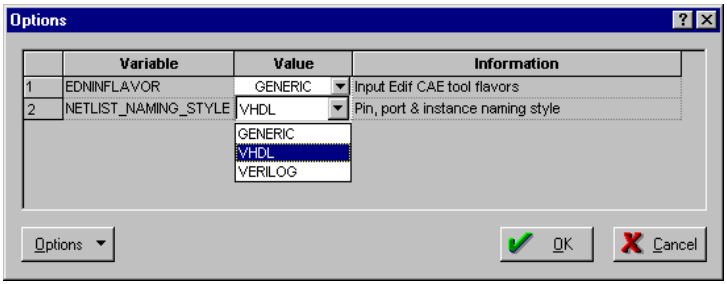

Figure 6-3. Read Netlist Options dialog box

7. **Select VHDL from the value pull-down menu, as shown in Figure 6-3.** Click OK.
8. **In the Read Netlist dialog box, click Open.** Confirmation that your netlist is opened is displayed in the Silicon Expert Window.

9. **Select the Design Report command from the Tools Menu.** This invokes the Design Reports Variables dialog box as shown in Figure 6-4.

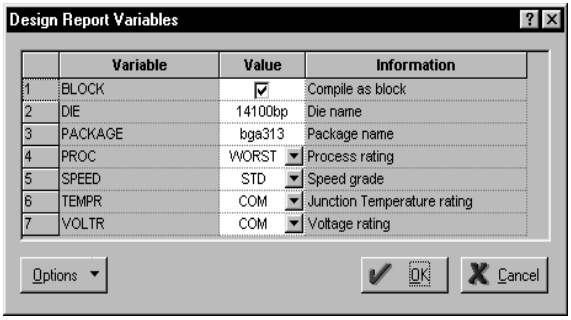

Figure 6-4. Design Report Variables dialog box

Generating a Netlist Report for a Block

You can run Design Report in block mode for a brief display of the timing estimates without the tool checking for I/O pads on the top level ports.

To turn on the Block Compiler and compile your netlist:

1. **Click the Design Report button on the Shortcut toolbar, as shown in Figure 6-5.**

Figure 6-5. Design Report Button

This displays the Design Report Variables dialog box, as shown in Figure 6-6.

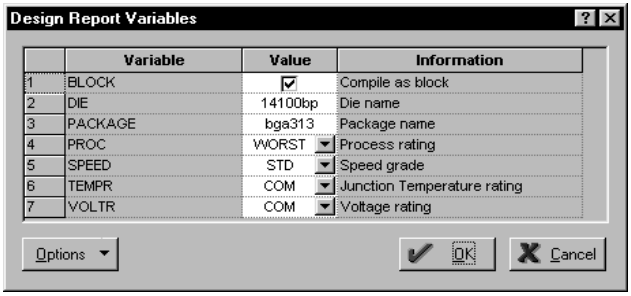

Figure 6-6. Design Report Variables dialog box

2. **Check the Block (Block Compile) in the Value column, as shown in Figure 6-6.** Click OK. A complete report of the netlist is displayed, including sequential and total logic utilization, operating conditions, inpad to register, register to register, register to outpad, inpad to outpad, and global signal propagation delays, and logic levels. The software automatically recognizes the global signals from the netlist.

Setting I/O Buffers with I/O Macro Manager

This section describes how to use the I/O Macro Manager tool to set I/O buffer assignments and specify global networks in the design.

To Use I/O Macro Manager:

1. **Select the I/O Macro Manager command from the Tools menu or the Shortcut toolbar.** This displays the I/O Macro Manager dialog box, as shown in Figure 6-7.

Figure 6-7. I/O Macro Manager dialog box

Examine the Current I/O column to see what type of buffers the software suggests. The signals “lnkclk” and “lnkres_l” are automatically recognized as global signals, by suggesting the use of clkbuf macros.

You can not assign macros that are illegal for a particular network. For example, both of the global signals in this design drive non-sequential macros, so the HCLK is not an I/O option.

2. **Click Ok, and observe the changes to the design in the Silicon Expert window.**

Saving a Modified Netlist

This section shows you how to save a modified netlist.

To save your netlist:

1. **Click the Write Netlist button on the Shorcut toolbar, as shown in Figure 6-8.** This invokes the Write Netlist dialog box. as shown in Figure 6-9. .

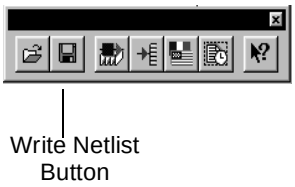

Figure 6-8. Write Netlist button

2. **In the File Name text box, change the name to c25bus_io.edn, as shown in Figure 6-9.** Click Save.

Figure 6-9. Write Netlist dialog box

Note: You will use this saved file in the next section of the tour.

Generating a Design Report

This section describes how to run a report on the design you completed and saved as c25bus_io.edn in the previous section.

To invoke Design Report:

1. **Click the Design Report button in the toolbar, as shown in Figure 6-10.**

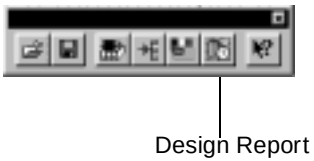

Figure 6-10. Design Report

This displays the Design Report Variables dialog box, as shown in Figure 6-11.

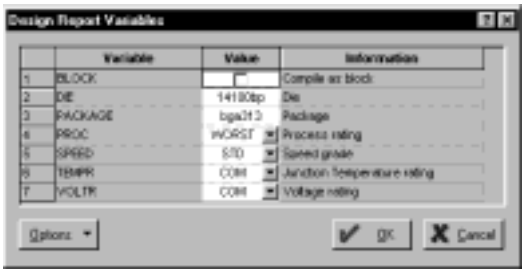

Figure 6-11. Design Report Variables dialog box

2. **Deselect the Block (Block Compile) check box.** Click OK, and observe the contents of the Silicon Expert window. Observe I/O and clock utilization for this design, and timing estimates in the Silicon Expert window for inpad to gated, inpad to clock, inpad to async, inpad to outpad, clkbuf to outpad, clock to outpad, and register to register.

Using The Buffer Manager Options

This section describes how to use the Buffer Manager options on the netlist C25bus_io.edn to balance buffer trees or correct fanout violations.

To invoke Buffer Manager:

1. **Select the Buffer Manager command from the Tools menu.** This action displays the Buffer Manager dialog box, as shown in Figure 6-12..

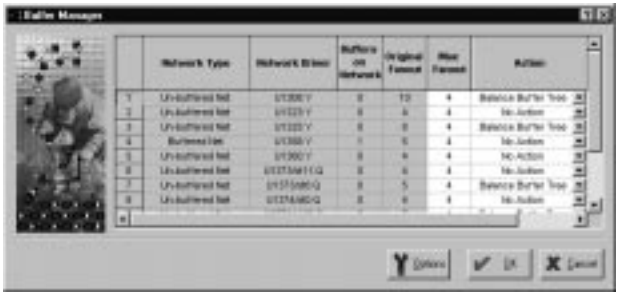

Figure 6-12. Buffer Manager dialog box

2. **Click the options button in the Buffer Manager dialog box.** This displays the Buffer Manager Options dialog box, as shown in Figure 6-13.

Figure 6-13. Buffer Manager Options dialog box

3. **Set Global Max fanout to 4, and Minimum Size for Network to 4.** Click OK.

The Buffer Manager dialog box is displayed, as shown in Figure 6-14, showing a list of all the macros that drive a network with a fanout greater or equal to 4.

In the Action column, actions that are recommended by the software are displayed. For example, the network driver from "U1308:Y" has a fanout of 10, which is greater than the Global Max Fanout of 4, so the recommended action is to balance the buffer tree.

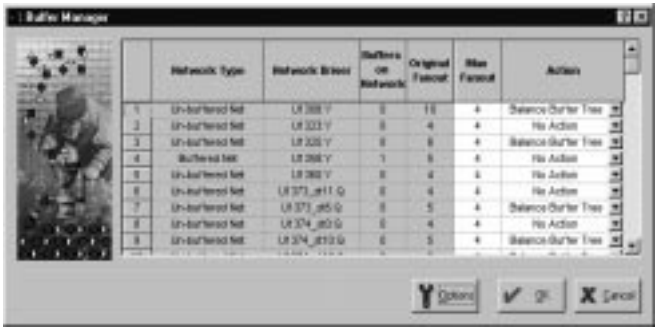

Figure 6-14. Buffer Manager dialog box

4. **Click OK to accept the defaults.** In the Silicon Expert window, the networks that were edited are displayed.

Observing Changes Implemented by Buffer Manager

This section describes how to observe the fanout and buffer changes implemented by Buffer Manager to the c25bus_io.edn design.

To see changes made by Buffer Manager:

1. **Select the Buffer Manager command from the Tools menu.** This displays the Buffer Manager dialog box, as shown in Figure 6-15.

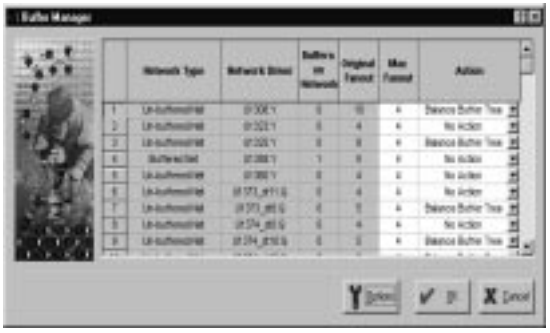

Figure 6-15. Buffer Manager dialog box

Observe the changes that have been implemented. The buffers on Network column now read 6 for the network driven by U1308:Y. Since this is a hierarchical design, the buffering is done by considering a pin of a hierarchical block to be a load of one. Buffers are therefore inserted at each hierarchical port in addition to what is needed to balance the tree.

Saving The Netlist

If you wish to preserve the changes made in Buffer Manager, you can save the netlist.

To re-name and save the netlist:

1. **Click the Write Netlist button in the toolbar, as shown in Figure 6-16.**

Figure 6-16. Write Netlist button

This invokes the Write Netlist dialog box, as shown in Figure 6-17.

Figure 6-17. Write Netlist dialog box

2. **In the File Name text box, change the name to c25bus_io_buf.edn.** Click Save.

Flattening a Netlist

For some applications, you may wish to remove the hierarchy in a design, and save it as a flat netlist. You can perform the following steps to flatten a netlist.

Opening the Previous Netlist

For this example, the netlist previously saved as c25bus_io.edn will be opened, and then flattened, using the Write Netlist Options.

To Open the c25bus_io.edn netlist:

1. **Click the Read Netlist button in the toolbar, as shown in Figure 6-18.** This invokes the Read Netlist dialog box as shown in Figure 6-19 on page 34.

.

Read Netlist Button

Figure 6-18. Read Netlist button

2. **Select the file c25bus_io.edn. Click Open.**

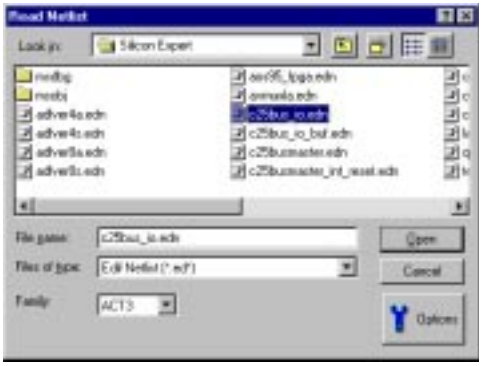

Figure 6-19. Read Netlist dialog box

Flattening the Netlist using Write Netlist Options

The c25bus_io.edn netlist will be flattened and saved using the Write Netlist option.

To invoke the Write Netlist dialog box:

1. **Click the Write Netlist button in the toolbar, as shown in Figure 6-20.**

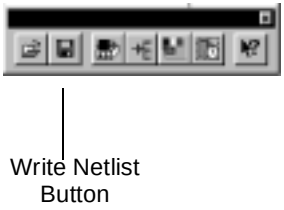

Figure 6-20. Write Netlist button

This invokes the Write Netlist dialog box, as shown in Figure 6-21.

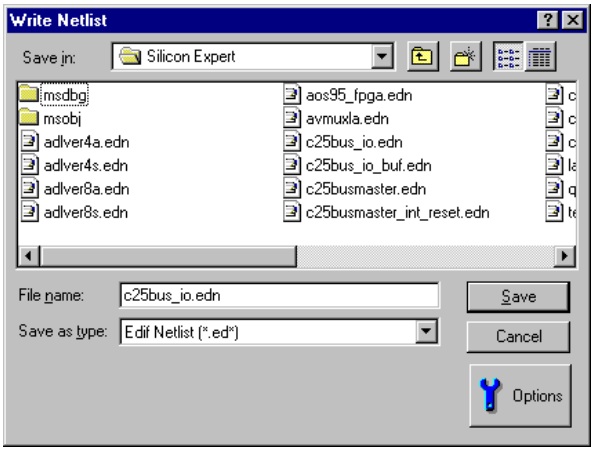

Figure 6-21. Write Netlist dialog box

2. **Click the Options button.** This displays the Write Netlist Options dialog box, as shown in Figure 6-22.

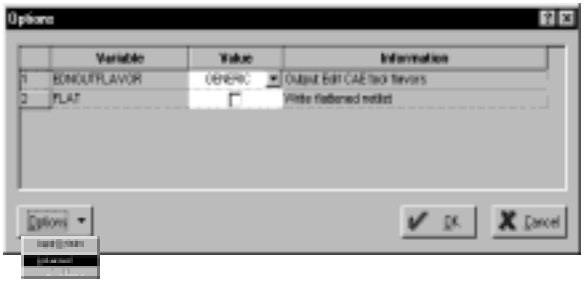

Figure 6-22. Write Netlist Options dialog box

3. **Click the options pull-down and select advanced, as shown in Figure 6-22.** This displays advanced features of the Write Netlist Options dialog box, as shown in Figure 6-23.

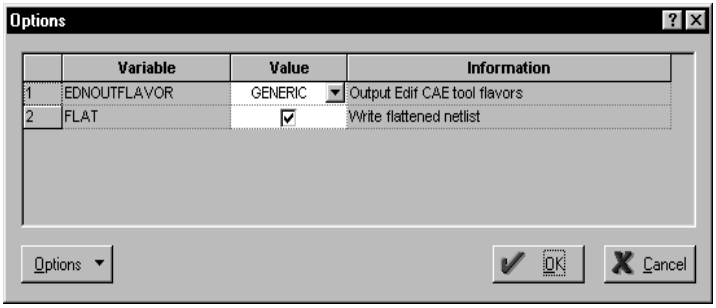

Figure 6-23. Write Netlist Options with Advanced Features Enabled

4. **Check the Flat checkbox.** This enables the flatten netlist feature, as shown in Figure 6-23. Click OK.

5. **In the File Name text box, change the name to c25bus_io_flat.edn, as shown in Figure 6-24.** Click OK. This creates a flat EDIF netlist.

Figure 6-24. Write Netlist dialog box

Using Buffer Manager to Change Fanout of the Design

You can use the Buffer Manager to change the global fanout of the non-hierarchical design in memory from the previous steps, as follows:

To invoke the Buffer Manager tool:

1. **Select the Buffer Manager command from the Tools menu.** This displays the Buffer Manager dialog box, as shown in Figure 6-25.

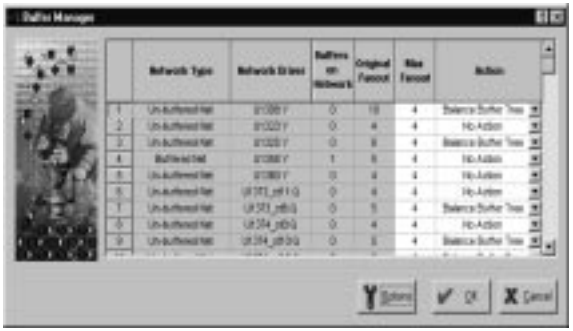

Figure 6-25. Buffer Manager dialog boxdialog box

2. **Click the Options button in the Buffer Manager dialog box.** This displays the Buffer Manager Options dialog box, as shown in Figure 6-13.

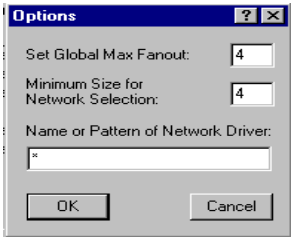

Figure 6-26. Buffer Manager Options dialog box

3. **Ensure that Global Max fanout is set to 4, and Minimum size for Network Selection is set to 4, as shown in Figure 6-26.** Click OK.
4. **Accept the defaults in the Buffer Manager dialog box.** Click OK.

Saving a Log File of Your Session

This section describes how save a text log file of your session.

To save a log file:

1. **Select the Save Report As command from the File Menu.** This invokes the Export Report dialog box, as shown in Figure 6-27. Navigate to a directory, specify a file name, and click Save.

Figure 6-27. Export Report dialog box

You can refer to this text file and view the actions that you have performed to see the current state of your netlist.

A

Menus, Commands, and Shortcut Toolbar

Features of Silicon Expert can be invoked using Silicon Expert menus. This appendix describes Silicon Expert menus, commands, and the shortcut toolbar.

File Menu

The File menu is shown in Figure A-1.

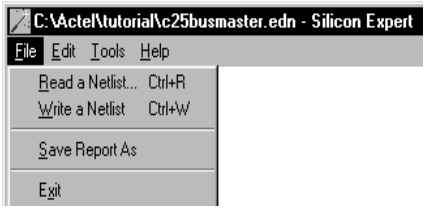

Figure A-1. File Menu

Read Netlist

The Read a Netlist command invokes the Read Netlist dialog box. Refer to "Read Netlist Dialog Box" on page 45 for more information about the Read Netlist dialog box.

Write Netlist

The Write a Netlist command invokes the Write a Netlist dialog box. Refer to "Write Netlist Dialog Box" on page 49 for more information about the Write Netlist dialog box.

Save Report As

The Save Report As command allows you to save a report as a .rpt file, using your netlist name or a name other than your netlist. Refer to "Design Report" on page 15 for more information about reports generated by Silicon Expert.

Exit

The Exit command allows you to exit Silicon Expert.

Edit Menu

The Edit menu is shown in Figure A-2.

Figure A-2. Edit Menu

Clear

The Clear command clears the information displayed on the Silicon Expert window. Refer to “Overview of Silicon Expert” on page 2 for more information about the Silicon Expert window.

Tools Menu

The Tools menu is shown in Figure A-3.

Figure A-3. Tools menu

Translate

The Translate command invokes the Translate Function of Silicon Expert. Refer to “Translate” on page 13 for more information about Translate.

Design Report

The Design Report command invokes the Design Report function of Silicon Expert. Refer to “Design Report” on page 15 for more information about Design Report.

I/O Macro Manager

The I/O Macro Manager command invokes the I/O Macro Manager dialog box. Refer to "I/O Macro Manager Dialog Box" on page 6 for more information about the I/O Macro Manager dialog box.

Buffer Manager

The Buffer Manager command invokes the Buffer Manager dialog box. Refer to Figure 3-1 on page 10 for more information about the Buffer Manager dialog box.

Help Menu

The Help menu is shown in Figure A-4.

Figure A-4. Help Menu

Help Topics

The Help Topics command invokes the Silicon Expert On-Line Help. Refer to "Actel Manuals" on page viii in the Introduction chapter for more information about On-Line Help.

About Silicon Expert

The About Silicon Expert command lists information about this release of Silicon Expert.

Silicon Expert Shortcut Toolbar

A shortcut toolbar is located on the Silicon Expert window. By clicking the buttons on the shortcut toolbar, you can invoke functions of Silicon Expert. The Silicon Expert shortcut toolbar is shown in Figure A-5.

Figure A-5. Silicon Expert Shortcut Toolbar

Read a Netlist Button

The Read Netlist button invokes the Read Netlist dialog box. Refer to for more information about the Read Netlist dialog box.

Write a Netlist Button

The Write a Netlist button invokes the Write a Netlist dialog box. Refer to “Write Netlist Dialog Box” on page 49 for more information about the Write a Netlist dialog box.

Silicon Expert Feature Buttons

Silicon Expert offers buttons to make it it easier to invoke the I/O Macro Manager, Buffer Manager, Translate, and Design Report functions. Silicon Expert buttons are shown in Figure A-6.

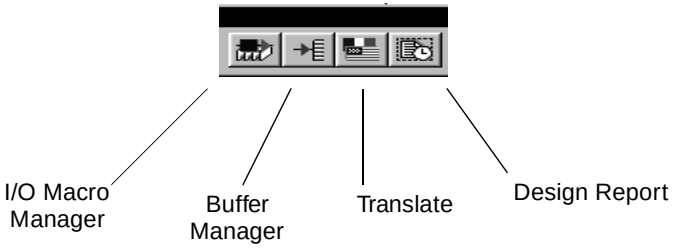

Figure A-6. Silicon Expert Buttons

Help Button

The Help button invokes Silicon Expert context-sensitive on-line help. After clicking this button, place the cursor over any item of a screen in Silicon Expert, and click again. A help topic appears with information about the item. Refer to “Actel Manuals” on page viii for more information about Silicon Expert on-line help.

B

Read Netlist Dialog Box

This appendix describes the Read Netlist dialog box and its options.

When you select Read a Netlist from the File menu or Translate from the Tools menu, the Read Netlist dialog box is displayed. The Read Netlist dialog box is shown in Figure B-1.

In the File Name box, enter the name of the netlist you wish to open, or use the Files of Type box to select the type of netlist file you wish to open (EDIF, Verilog, or ADL), and use the Look In box to navigate to the desired .edn file.

In the Family box, select the Actel device family from the pull-down menu. Click Open to open the netlist.

Figure B-1. Read Netlist dialog box

Read Netlist Options Dialog Box

The Read Netlist Options dialog box is displayed when you click the Options button, located at the lower right of the Read Netlist dialog box. The options are available when EDIF or ADL is selected in the File of Type box. The Read Netlist Options dialog box is shown in Figure B-2.

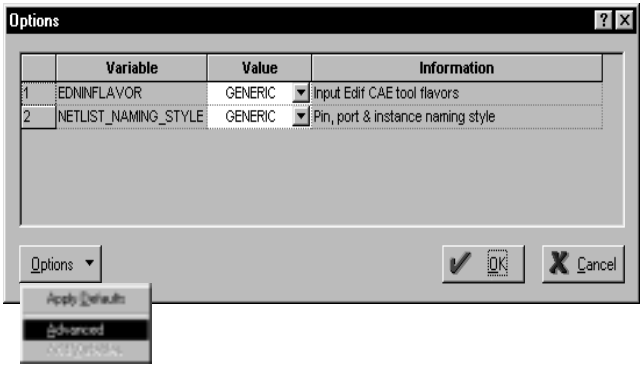

Figure B-2. Read Netlist Options dialog box

The following are descriptions of the Read Netlist Options spreadsheet columns.

Variable Column

The Variable column lists the variables that control the netlist reader.

Value Column

The Value column displays values that can be changed and applied for a netlister variable. You can double-click check boxes, select commands from drop down menus, or fill in blanks to modify displayed values.

Information Column

The Information column displays a brief description of the variable and its function.

Additional Read Netlist Options

Additional options are displayed in the pull down menu in the lower left portion of the Read Netlist dialog box (Figure B-2. The following are descriptions of the additional option selections.

Apply Defaults

When you click the Apply Default option, the values in the Netlist Options spreadsheet are reset to the default values.

Advanced

When you click the Advanced option, additional netlister variables are displayed that allow advanced users more control over the netlister read operation.

Add Variables

When you click the Add Variables option, you can add undocumented netlister variables.

C

Write Netlist Dialog Box

This appendix describes the Write Netlist dialog box and its options.

After a design is optimized with I/O Macro Manager, Buffer Manager, or Translate, you can write an optimized netlist file, which can be read into the Designer software for design implementation. The Write Netlist dialog box is shown in Figure C-1.

In the File Name box, enter the name of the netlist you wish to save, or use the Save as Type box to select the type of netlist file you wish to save (EDIF, Verilog, VHDL, or ADL), and use the Save In box to navigate to the desired directory in which to save your netlist file. Click Save to save the netlist.

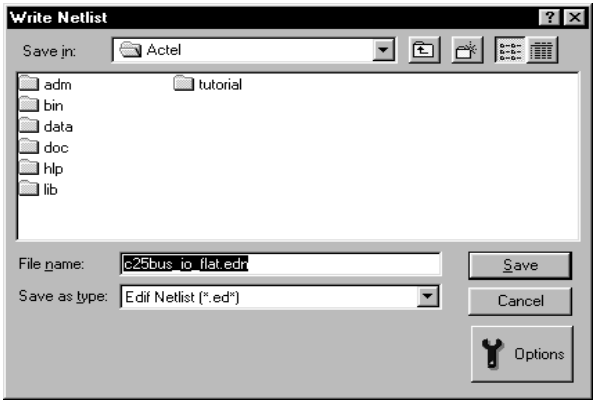

Figure C-1. Write Netlist Dialog Box

Write Netlist Options Dialog Box

The Write Netlist Options dialog box is displayed when the Options button, located at the lower right of the Write Netlist dialog box, is clicked. The options are available when EDIF or ADL is selected in the

File of Type box. The Write Netlist Options dialog box is shown in Figure C-2.

Figure C-2. Write Netlist Options Dialog Box

The following are descriptions of the Write Netlist Options spreadsheet columns.

Variable Column

The Variable column lists the variables that control the netlist reader.

Value Column

The Value column displays values that can be changed and applied for a netlister variable. You can click check boxes, select commands from drop down menus, or fill in blanks, as needed, to modify displayed value.

Information Column

The Information column displays a brief description of the variable and its function.

Additional Write Netlist Options

Additional options are displayed in the pull down menu in the lower left portion of the Write a Netlist Options dialog box. The following are descriptions of the additional option selections.

Apply Defaults

When you click the Apply Default option, the values in the Netlist Options spreadsheet are reset to the default values.

Advanced

When you click the Advanced option, additional netlister variables are displayed which allow advanced users more control over the netlister read operation.

Add Variables

When you click the Add Variables option, you can add undocumented netlister variables.

D

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a Web and FTP site, electronic mail, and worldwide sales offices. This appendix contains information about using these services and contacting Actel for service and support.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel Toll-Free Line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
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Customer Applications Center

The Customer Applications Center is staffed by applications engineers who can answer your hardware, software, and design questions.

All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Guru Automated Technical Support

Guru is a Web based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations and links to other resources on the Actel Web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources we have provided on the net.

Be sure to visit the "Actel User Area" on our Web site, which contains information regarding: products, technical services, current manuals, and release notes.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. You can directly obtain library updates, software patches, design files, and data sheets.

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. The e-mail account is monitored several times per day.

The technical support e-mail address is **tech@actel.com**.

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