MOTIVE™ Static Timing Analysis

Interface Guide

Actel

UNIX® Environments

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Trademarks

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Introduction

The *MOTIVE Static Timing Analysis Interface Guide* contains information about using MOTIVE software to perform timing analysis on Actel designs. Refer to the *Designing with Actel* manual for information about using the Designer Series FPGA development software tools and the Viewlogic *MOTIVE User's Guide* for additional information about using the MOTIVE static timing analysis tool.

Document Organization

The *MOTIVE Static Timing Analysis Interface Guide* is divided into the following chapters:

Chapter 1 - Setup contains information and procedures about setting up the MOTIVE static timing analysis tool to analyze Actel designs.

Chapter 2 - Design Flow illustrates and describes the design flow for analyzing Actel designs using the MOTIVE static timing analysis tool.

Chapter 3 - Timing Analysis contains information and procedures about performing timing analysis on Actel designs with MOTIVE.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

The information in this manual is based on the following assumptions:

1. You have installed the Designer Series software.
2. You have installed the MOTIVE software.
3. You are familiar with UNIX workstations and operating systems.
4. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The contents of a file is formatted as follows:

```
file contents
```

Messages that are displayed on the screen appear as follows:

```
Screen Message
```

The <act_fam> variable represents an Actel device family. To reference an actual family, substitute the name of the Actel device when you see this variable. Available families are act1 (for ACT 1 and 40MX devices), act2 (for ACT 2 and 1200XL devices), act3, 3200dx (for 3200DX and 42MX devices), and 54sx.

Actel Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the on-line manuals, you must install Adobe® Acrobat Reader® from the CD-Rom.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

DeskTOP Interface Guide. This guide contains information about using the integrated VeriBest® and Synplicity® CAE software tools with the Actel Designer Series FPGA development tools to create designs for Actel Devices.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic Powerview® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

Actel FPGA Data Book. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

On-Line Help

The Designer Series software comes with on-line help. On-line help specific to each software tool is available in Designer, ACTgen, ACTmap, Silicon Expert, Silicon Explorer, Silicon Sculptor, and APSW.

1

Setup

This chapter contains information about setting up the MOTIVE static timing analysis tool to analyze Actel designs. Refer to the *MOTIVE User's Guide* for additional information about installing and setting up MOTIVE.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R1-1999 or later and the MOTIVE static timing analysis tool. For specific information about which versions are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

System Setup

After installing MOTIVE, make sure the proper environment variables are set in your UNIX shell script. The following are C shell variables. If you are using another shell, adjust the syntax accordingly.

```
setenv ALSDIR /<actel_install_directory>
setenv QUADHOME /<motive_install_directory>
setenv QUADBIN /<motive_executable_directory>
setenv XLNSPATH $QUADHOME/X11/nls
```

If you are using SunOS or Solaris, the following variable must also be set:

```
setenv LD_LIBRARY_PATH $ALSDIR/lib
```

If you are using HP-UX, the following variable must also be set:

```
setenv SHLIB_PATH $ALSDIR/lib
```

Refer to the *Designing with Actel* manual and the Viewlogic documentation for additional information about setting environment variables.

Actel MOTIVE Libraries

The Actel MOTIVE libraries contain standard MOTIVE models for Actel hard and I/O macros. These libraries can be used for SDF back annotation of interconnect and pin-to-pin delays and pre-layout and post-layout analysis using a Designer SDF file.

The libraries are installed in the "$ALSDIR/lib/motive/<act_fam>" directories.

2
Design Flow

This chapter illustrates and describes the design flow for performing timing analysis on Actel designs using the MOTIVE static timing analysis tool. Refer to the *Designing with Actel* manual for additional information about the design flow for creating Actel designs.

Design Flow Illustrated

Figure 2-1 shows the design flow for performing static timing analysis on an Actel design using the MOTIVE and Designer Series software[1].

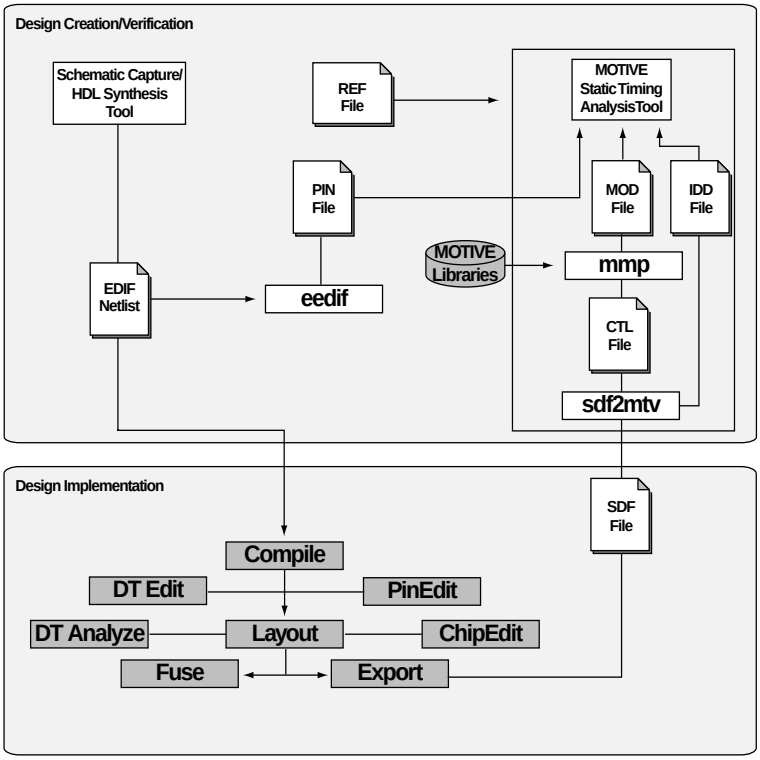

Figure 2-1. Actel-MOTIVE Static Timing Analysis Design Flow

1. Actel-specific utilities/tools are denoted in grey in Figure 2-1.

Design Flow Overview

The Actel-MOTIVE design flow has three main steps; design creation/ verification, design implementation, and timing analysis. These steps are described in the following sections.

Design Creation/ Verification

During design creation/verification, an HDL or schematic-based design is created. After creating the design, an EDIF netlist is generated for use in generating necessary MOTIVE files.

Design Creation

Create your design using an HDL or schematic capture CAE tool. Refer to the *Designing With Actel* manual and the documentation included with your CAE tool for information about creating a design.

EDIF Netlist Generation

After you have created your design, generate an EDIF netlist for use in Designer. Refer to the documentation included with your CAE tool for information about generating an EDIF netlist.

Design Implementation

During design implementation, a design is placed and routed using Designer. After place and route, an SDF file is exported from Designer. Additionally, MOTIVE files are generated and timing analysis is performed on a design using MOTIVE.

Place and Route

Use Designer to place and route your design. Make sure you specify GENERIC as the Edif Flavor and Generic as the naming style when importing the EDIF netlist. After placing and routing the design, export an SDF file for use in generating MOTIVE files. Refer to the *Designing With Actel* manual for information about using Designer.

MOTIVE File Generation

The “sdf2mtv” utility (provided with MOTIVE) reads the SDF file and produces the control (CTL) and the interconnect delay (IDD) files. The “mmp” utility reads the CTL file and the Actel MOTIVE libraries to generate a model (MOD) file of the design to be used for timing

analysis with MOTIVE. The “eedif” utility translates the EDIF netlist into a MOTIVE pin (PIN) file to be used for static timing analysis. Refer to “Generating Files for Timing Analysis” on page 7 and the *MOTIVE User’s Guide* for information about generating MOTIVE files.

Timing Analysis

Use the MOTIVE static timing analysis tool to perform static timing analysis on your design. Refer to Chapter 3, “Setting Up MOTIVE for Static Timing Analysis” on page 9 and the *MOTIVE User’s Guide* for information about performing timing analysis.

3

Static Timing Analysis

This chapter describes the procedure for generating the necessary files and setting up MOTIVE to perform static timing analysis on an Actel design. Refer to the Viewlogic *MOTIVE User's Guide* for information about performing timing analysis.

Generating Files for Timing Analysis

The MOTIVE tool requires several files to perform static timing analysis. This section describes the files and the procedures for generating those files.

EDIF Netlist

The EDIF netlist is generated by your CAE tool and is used in Designer to generate timing information and a MOTIVE netlist. Refer to the documentation included with your CAE tool for information about generating an EDIF netlist.

SDF 2.1 File

The SDF 2.1 file is exported from Designer and contains timing information. The file is used to generate an interconnect delay file. Use the following procedure to export an SDF 2.1 file:

1. **Invoke Designer.**
2. **Import your EDIF netlist.** Choose Import Netlist File from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC as the Edif Flavor, and Generic as the Naming Style. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.
3. **Compile your Design.** Choose the Compile command from the Tools menu or click the Compile button.
4. **Export an SDF file.** Choose the Export command from the File menu. The Export dialog box is displayed. Choose Timing File as the File Type, and SDF 2.1 as the Format. You can export pre-layout or post layout timing information for use in MOTIVE.

Pre-Layout Timing

Check the Pre-Layout Timing box and click OK. Designer exports the pre-layout timing information.

Post-layout Timing

Make sure the Pre-Layout Timing box is not checked and click OK. Designer places and routes the design then exports the post-layout timing information.

Pin (PIN) File

The PIN file is generated from the EDIF netlist. The file is a MOTIVE netlist. To generate a PIN file, type the following command at the prompt:

```
eedif -pin -log -c UP -names ORIGINAL <design_name>.edn
```

The “eedif” program generates a“<design_name>.pin” file in the current directory.

Reference (REF) file

The REF file is a text file that provides MOTIVE with clock reference information including clock groups, clock skew, multicycle path information, etc. You must create the REF file manually before performing analysis. Refer to the Viewlogic *MOTIVE User’s Guide* for information about creating a reference file. The following is an example REF file:

```
## Reference file for Sample Circuit
GROUP A
REF CLK T
CYDEF UP 0. 0. DOWN 1. 1. CYCLE 2.
GROUP B
REFDEF CLKTEST T
CYDEF UP 0. 0. DOWN 1. 1. CYCLE 2.
# Min and Max Width of Clock High Period
ENDREF
# Clock Skew Matrix
CLKGEN A A -2. 2.
CLKGEN A B -4. 4.
CLKGEN B B -2. 2.
```

Interconnect Delay (IDD) File

The IDD file is generated from the SDF file in MOTIVE. The file contains interconnect delay information. Refer to step 7 in the following procedure for information about generating an IDD file.

Control (CTL) File

The CTL file is generated from the SDF file in MOTIVE. The file contains the intrinsic or pin-to-pin information. Refer to step 7 in the following procedure for information about generating a CTL file.

Model (MOD) File

The MOD file is generated from the CTL file in MOTIVE. The file contains the appropriate timing models with annotated intrinsic or pin-to-pin timing used in MOTIVE. Refer to step 8 in the following procedure for information about generating a MOD file.

Setting Up MOTIVE for Static Timing Analysis

Once you have generated the necessary files you can set up a project in MOTIVE to perform static timing analysis on an Actel design. Use the following procedure to setup MOTIVE:

1. **Invoke MOTIVE.** Type the following command at the prompt:

   ```
   motive
   ```

2. **Create a project for your design.** Click the Name tab in the Project window and type the name of your project in the Project name box. Click the Accept button. The Flow window tab is highlighted.
3. **Select flow type.** Click the Type tab in the Flow window. Choose the “ASIC - Using flat pin file and SDF” flow option. Click the Accept button. The Options window tab is highlighted.
4. **Set usage options (optional).** Click the Options window tab and set your usage options. Click the Accept button. Refer to the Viewlogic *MOTIVE User’s Guide* for information about setting usage options.

5. **Import your PIN file.** Click the Import tab in the PIN File window. Type the name of your PIN file in the Pinlist file box, and click the Load Netlist button. The MOTIVE Interaction Log and Tips window is displayed. Click the green OK button.

   Note: If the OK button is not green, you have errors in your PIN file. You must correct the errors before continuing.

6. **Run an incremental build.** Click the Check tab. Click the Incremental build button to check for errors. The MOTIVE Interaction Log and Tips window is displayed. Click the green OK button.

   Note: If the OK button is not green, you have errors. You must correct the errors before continuing.

7. **Generate an IDD file and a CTL file from the SDF.** Click the Translate tab in the SDF window. Type the name of your SDF file in the SDF file box. Change the name of the IDD and CTL files to match the name of your design. Click the Process SDF file button. The MOTIVE Interaction Log and Tips window is displayed. Click the green OK button.

   Note: If the OK button is not green, you have errors. You must correct the errors before continuing.

   This generates a “<design_name>.idd” and a “<design_name>.ctl” file in the “./mtv_sa” directory.

8. **Generate a MOD file from the CTL file.** Click the MMP tab. Enter the name of your CTL file in the Control box. Type the full hard path name location of the actel MOTIVE libraries in the Libraries box. Change the name of the MOD file and revised CTL file to match the name of your design. Click the Run MMP button. The Process Execution Log and Tips window is displayed. Click the green OK button.

   Note: If the OK button is not green, you have errors in your PIN file. You must correct the errors before continuing.

   This generates a “<design_name>.mod” file in the“./mtv_sa” directory using the “<design_name>.ctl” file and the Actel MOTIVE library.

9. **Run an incremental build.** Click the Check tab. Click the Incremental build button to check for errors. The MOTIVE Interaction Log and Tips window is displayed. Click the green OK button.

   Note: If the OK button is not green, you have errors. You must correct the errors before continuing.

10. **Import your REF file.** Click the File tab in the Clocks window. Type the name of your REF file in the Clock Reference file box. Click the Accept button.

11. **Run an incremental build.** Click the Incremental build window tab. Click the Incremental build button to check for errors. The MOTIVE Interaction Log and Tips window is displayed. Click the green OK button.

    Note: If the OK button is not green, you have errors. You must correct the errors before continuing.

12. **Refresh the MOTIVE database for your design.** Click the Finish window tab. Click the Build button.

13. **Perform static timing analysis.** Refer to the *MOTIVE User's Guide* for information about performing static timing analysis.

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a Web and FTP site, electronic mail, and worldwide sales offices. This appendix contains information about using these services and contacting Actel for service and support.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel Toll-Free Line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1256 305600.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

The Customer Applications Center is staffed by applications engineers who can answer your hardware, software, and design questions.

All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Guru Automated Technical Support

Guru is a Web based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations and links to other resources on the Actel Web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources we have provided on the net.

Be sure to visit the "Actel User Area" on our Web site, which contains information regarding: products, technical services, current manuals, and release notes.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. You can directly obtain library updates, software patches, design files, and data sheets.

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. The e-mail account is monitored several times per day.

The technical support e-mail address is **tech@actel.com**.

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