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PowerGauge with ModelSim

Agenda

- Power Estimation in Altera PLD
- PowerGauge™ Power Analysis in Quartus® II Software
- Quartus™ II Software/ ModelSim Overview
- Simulating with ModelSim
 - Timing Simulation
- Calculate Power in Quartus II Software



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Power Estimation in Altera PLD

Web-Based Power Calculator

- Easy to Use with Click
- Need to Input Value from Report After Compilation In Quartus II
- Support APEX 20KE/C & APEX™ II & Mercury™ Devices (Supporting Stratix™ Devices Soon)

APEX 20KE & 20KC Power Calculator Step 2: Enter Logic Array Information

<< Go back to Step 1

Go forward to Step 3 >>

Enter information in the calculators below.

- [Clock tree power consumption](#)
- [Logic element \(LE\) power consumption](#)
- [Embedded system block \(ESB\) power consumption](#)
- [General-purpose phase-locked loop \(PLL\) power consumption](#)

I_{CCINT} Standby (mA)
10

Clock Tree Power Consumption

Calculate

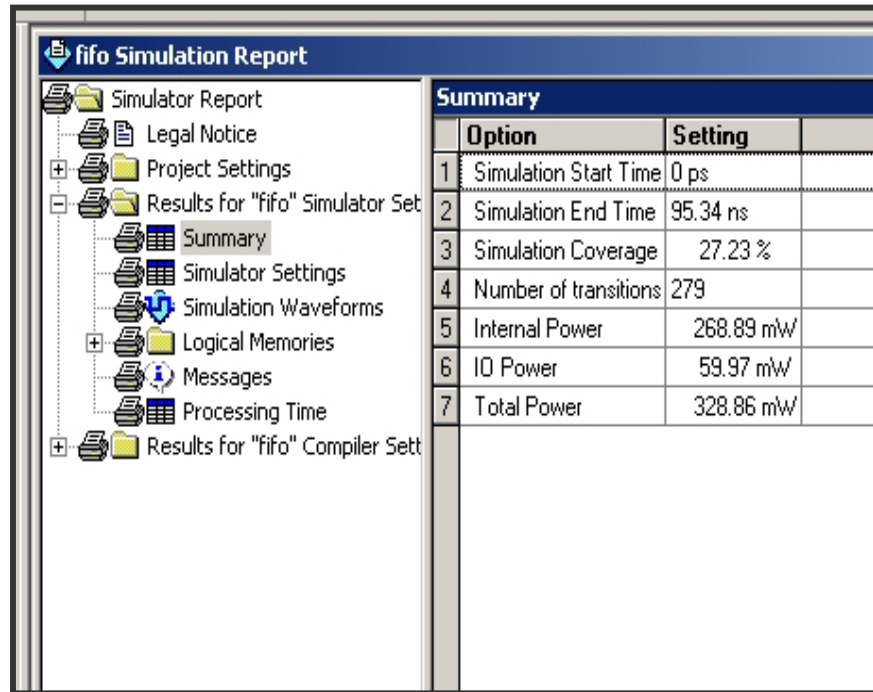
[\[Go to Top\]](#)

Dedicated Clocks	f _{MAX} (MHz)	Flip-Flops	I _{CCINT} (mA)	P _{INT} (mW)
1	50.00	4,000.00	91.92	165.46
2	0.00	0.00	0.00	0.00
3	0.00	0.00	0.00	0.00
4	0.00	0.00	0.00	0.00
Subtotal:			91.92	165.46

Fast Global Clocks	f _{MAX} (MHz)	Flip-Flops	I _{CCINT} (mA)	P _{INT} (mW)
1	0.00	0.00	0.00	0.00
2	0.00	0.00	0.00	0.00

Quartus II Power Calculator

- 1. Must Make Vector Wave Form File (*.vwf) for Using PowerGauge in Quartus II Software
- 2. More Accurate than Web Based Power Calculator
- 3. Support APEX Family & Mercury Devices (Supporting Stratix Devices in Next Version)



The screenshot displays the 'fifo Simulation Report' window. On the left is a tree view of the report contents, including folders for 'Simulator Report', 'Project Settings', 'Results for "fifo" Simulator Set', and 'Results for "fifo" Compiler Set'. The 'Summary' folder is expanded, showing a table of simulation metrics.

Summary	
Option	Setting
1	Simulation Start Time 0 ps
2	Simulation End Time 95.34 ns
3	Simulation Coverage 27.23 %
4	Number of transitions 279
5	Internal Power 268.89 mW
6	IO Power 59.97 mW
7	Total Power 328.86 mW



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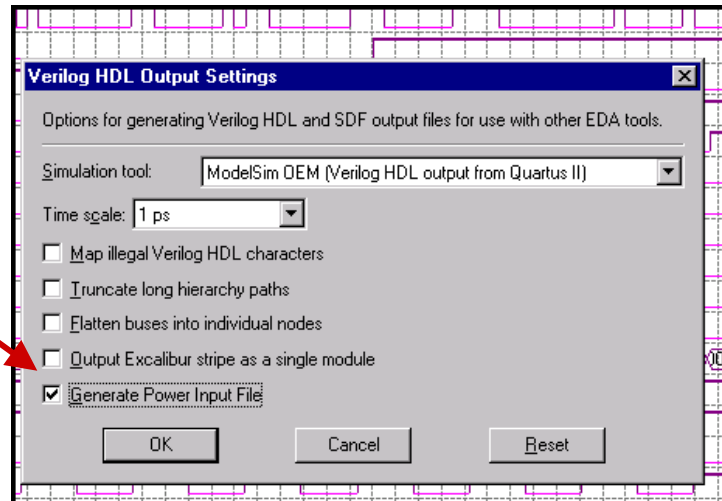
PowerGauge in Quartus II



PowerGauge Analysis Software

- Estimates Power Consumption Based on Toggle Rate
 - Toggle Rate Derived from User Generated Simulation Vectors
 - Use Quartus II Simulator
- Provides Support For Multiple I/O Standards
- Supports APEX 20KE & Mercury Families
- Modelsim Can Output .Pwf File That Can Be Read by the Quartus II Simulator

**Project >EDA Tool Settings
>Modelsim Settings
Generate Power Input File**



Power Analysis in Quartus II

Simulator Settings

General | Time/Vectors | Mode | Options

Select options for simulation. The setup/hold and glitch options are available only for a simulation that includes Compiler-generated timing information. Note: the availability of some options depends on the current device family.

Changes apply to Simulator settings 'filtref'

Simulation coverage reporting

Setup and hold time violation detection

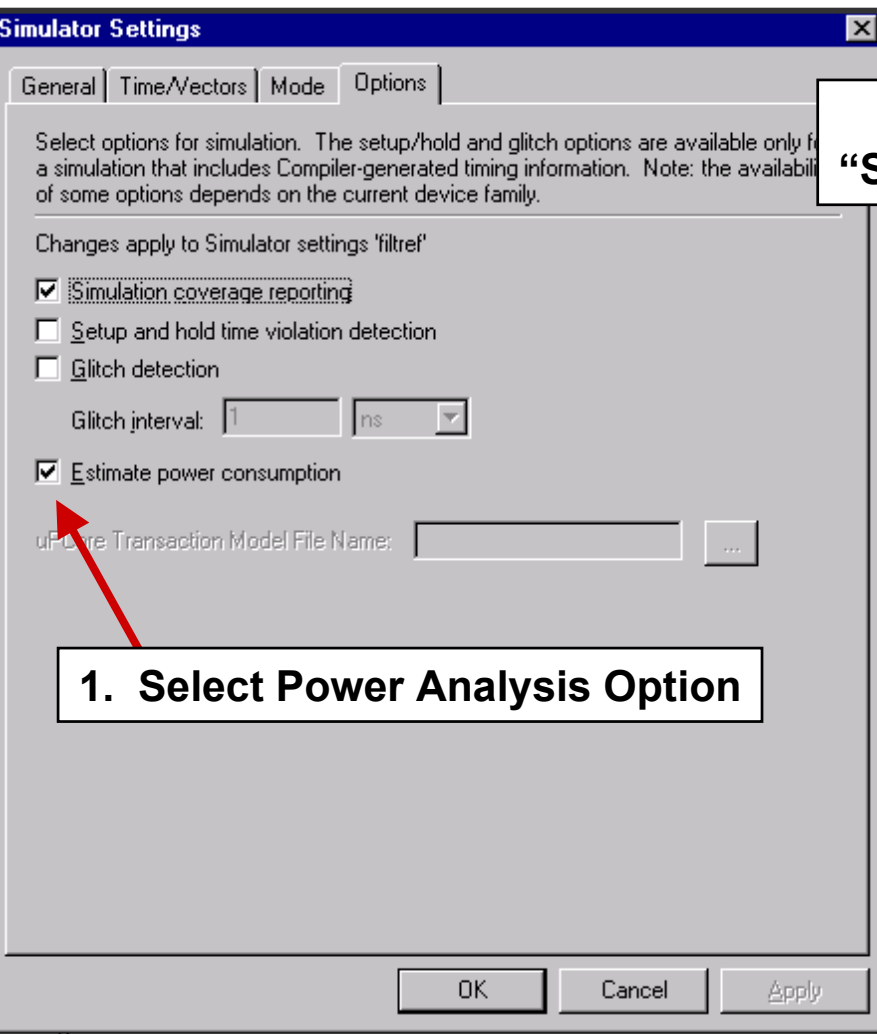
Glitch detection

Glitch interval: 1 ns

Estimate power consumption

UP Core Transaction Model File Name:

OK Cancel Apply



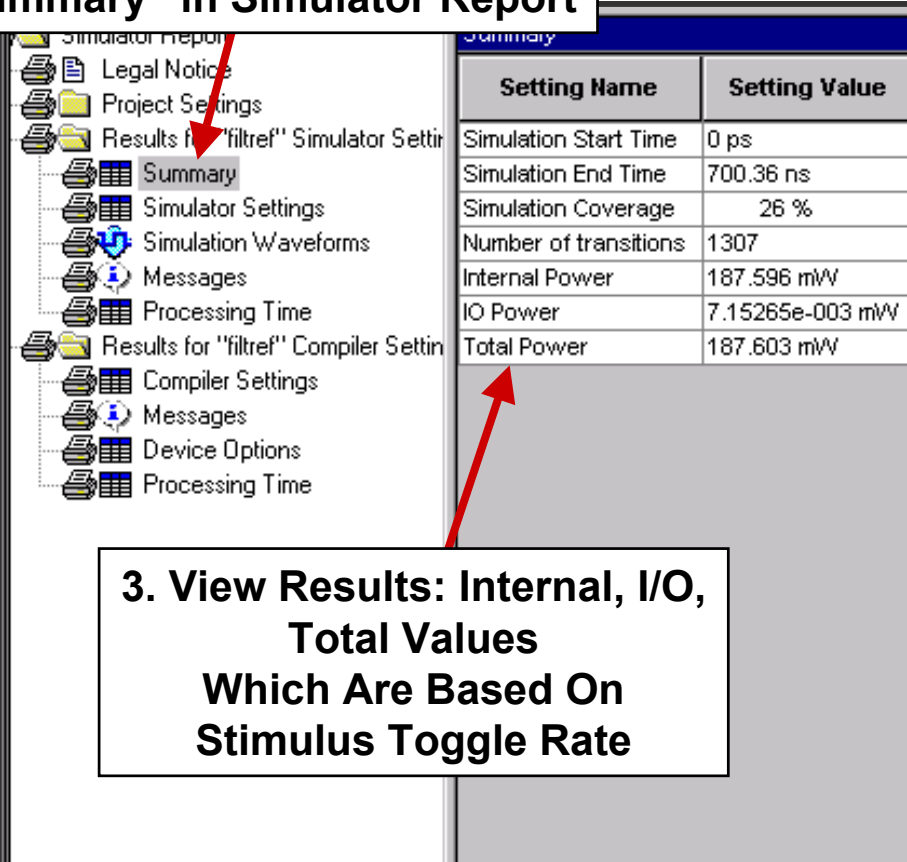
1. Select Power Analysis Option

2. Simulate & Select "Summary" in Simulator Report

Simulator Report

- Legal Notice
- Project Settings
- Results for "filtref" Simulator Settings
 - Summary**
 - Simulator Settings
 - Simulation Waveforms
 - Messages
 - Processing Time
- Results for "filtref" Compiler Settings
 - Compiler Settings
 - Messages
 - Device Options
 - Processing Time

Setting Name	Setting Value
Simulation Start Time	0 ps
Simulation End Time	700.36 ns
Simulation Coverage	26 %
Number of transitions	1307
Internal Power	187.596 mW
IO Power	7.15265e-003 mW
Total Power	187.603 mW



3. View Results: Internal, I/O, Total Values Which Are Based On Stimulus Toggle Rate



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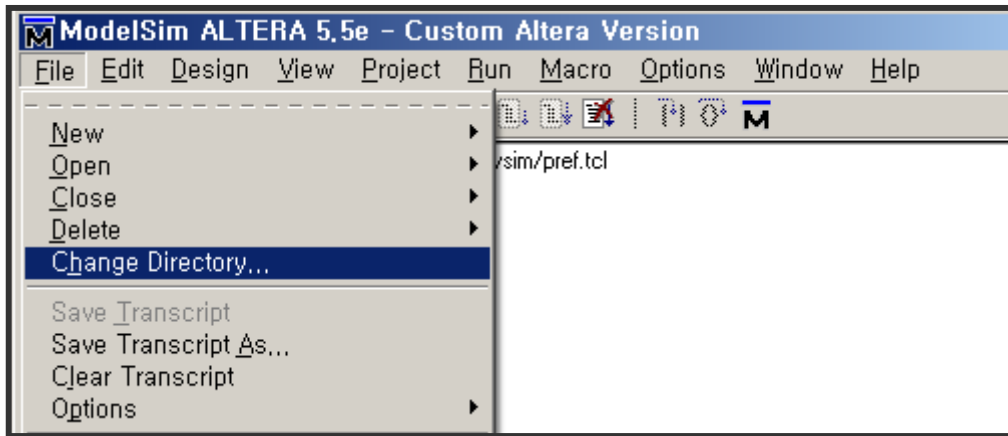
Quartus II/ ModelSim Overview



Basic Simulation Steps

- 1 ⇒ **Change Directory**
- 2 ⇒ **Create Library(s)**
- 3 ⇒ **Map Library to Physical Directory**
- 4 ⇒ **Compile Source Code**
 - All HDL Code Must Be Compiled
 - Different for Verilog & VHDL
- 5 ⇒ **Load Design**
- 6 ⇒ **Start Simulator**

1 ⇒ Change Directory



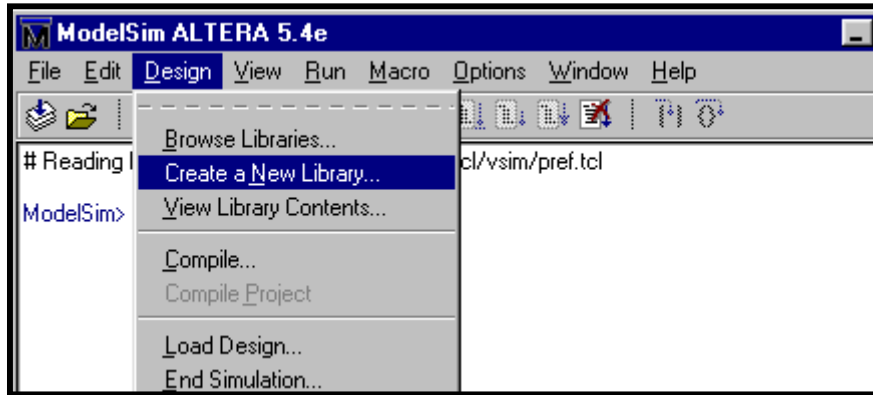
UI) From within Main Window:

File -> Change Directory

Cmd) From within Main, transcript window:

ModelSim> *cd <drive>:./<directory name>*

2 ⇒ Creating ModelSim Library(s)



UI) From within Main Window:

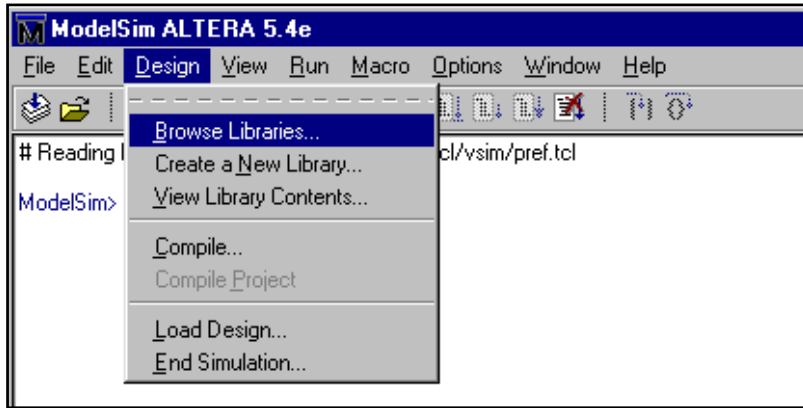
Design -> Create a New Library

Cmd) from within Main, transcript window:

ModelSim> vlib <library name>

3 ⇒ Map Logical Library Name(s)

- Syntax: *vmap* <logical_name> <directory_path>



UI) From within Main Window:

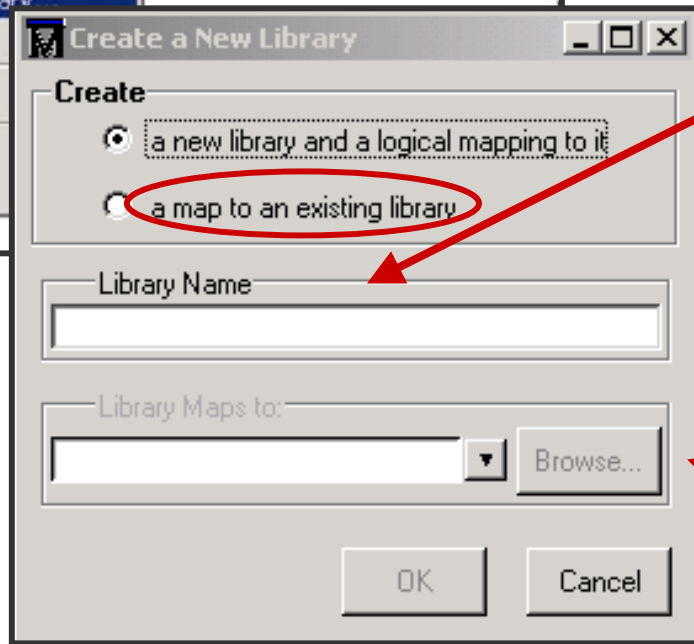
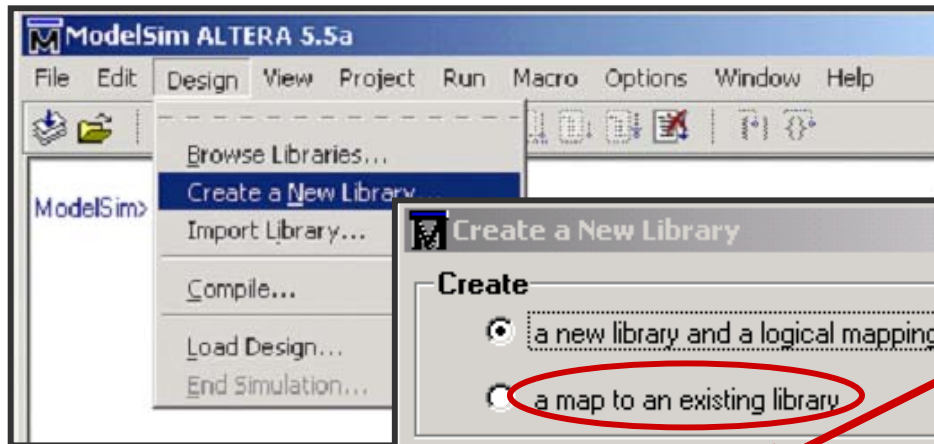
Design -> Browse Libraries

Design -> Create a New Library

Cmd) From within Main, Transcript Window:

```
ModelSim> vmap my_work c:\my_design\my_lib
```

Mapping Existing Libraries (UI)



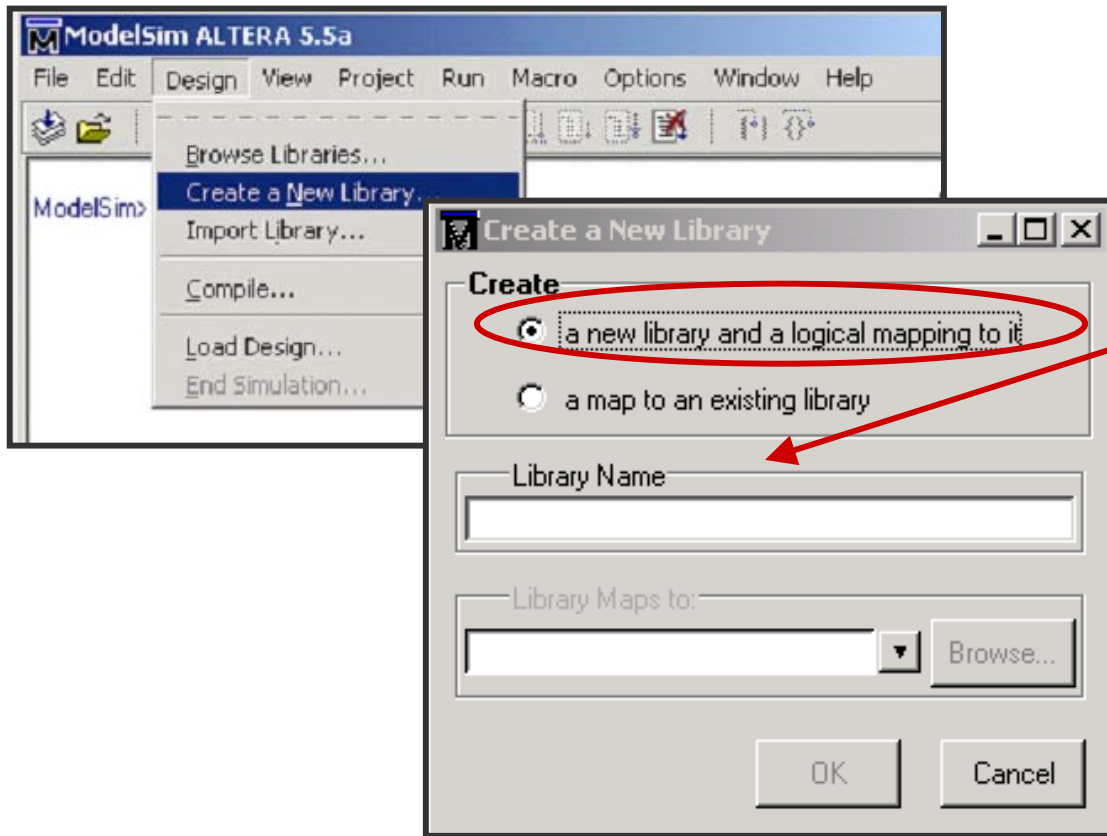
Select *Map To An Existing Library* & Type Library Name

Use This Command To Map to Library Directory of Pre-Compiled Design Units

Browse to Library Directory

```
-> vmap lpm_sim c:\QuartusII\library\lpm
```

Mapping Existing Libraries (UI)

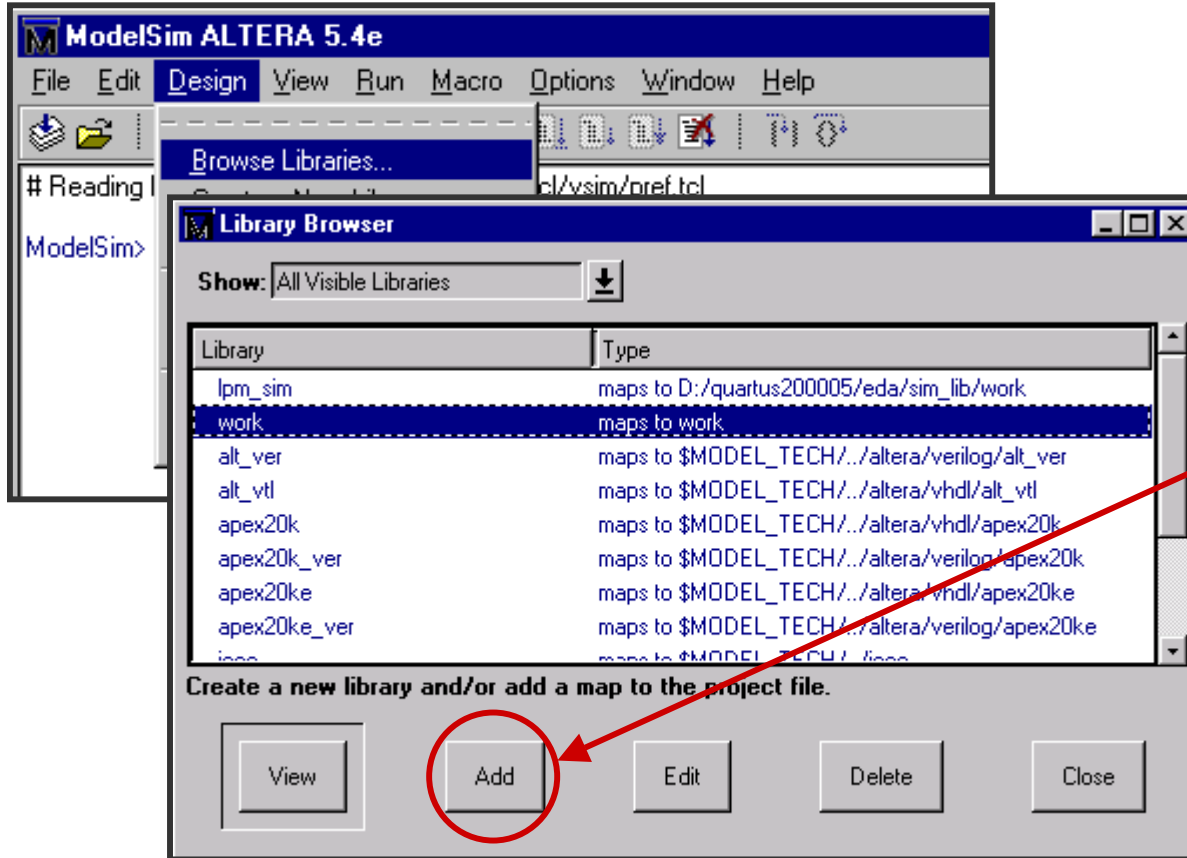


Select A New Library & A Logical Mapping to It & Type Library Name

This Command Creates Library Subdirectory in Local Directory & Then Sets Mapping for It

-> vlib my_lib
-> vmap my_lib my_lib

Mapping Libraries (UI)



Use **Add** Button to Create New Library & Map

4 ⇒ Compile Source Code (VHDL)

- UI) *Design -> Compile*
- Cmd) `vcom -work <library_name> <file1>.vhd <file2>.vhd`
 - Files Are Compiled in Order They Appear
 - Compilation Order/Dependencies (Next Slide)
- '87 VHDL is default
 - UI) Use Default Options button to set '93
 - Cmd) Use -93 Option (Must Be First Argument)
- Default Compiles into Library Work
 - Ex. `Vcom -93 my_design.vhd`

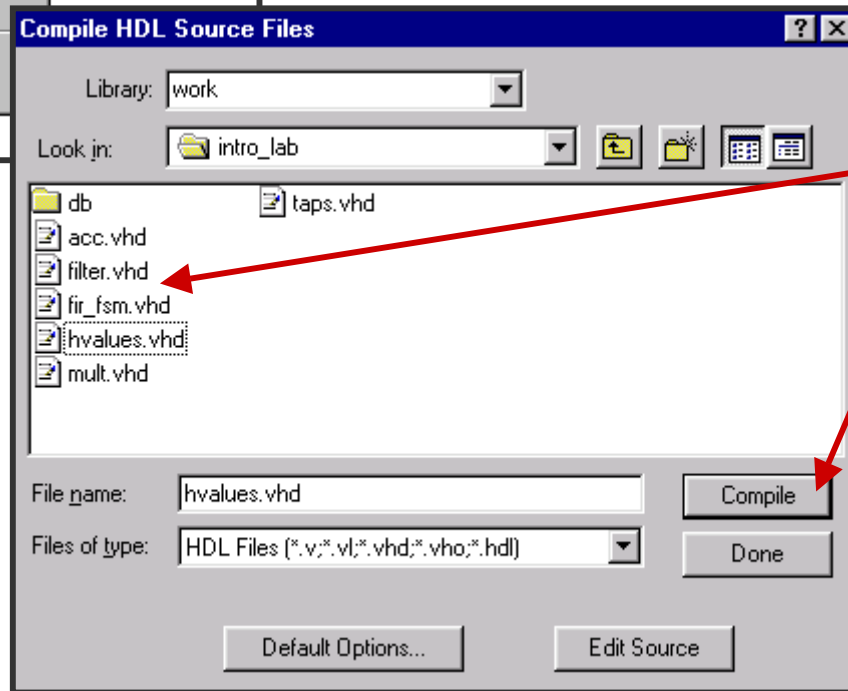
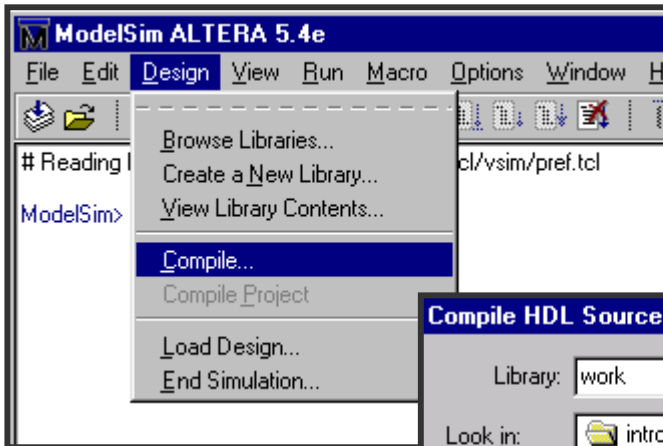
Note: Design Units Must Be Re-Analyzed When Design Units They Reference Are Changed in Library.

4 ⇒ Compile Source Code (Verilog)

- UI) *Design -> Compile*
- Cmd) `vlog -work <library_name> <file1>.v <file2>.v`
 - Files Are Compiled In Order They Appear
 - Order Of Files or Compilation Does Not Matter
- Supports Incremental Compilation
- Default Compiles Into Library Work
 - Ex. `vlog my_design.v`

Note: Design Units Must Be Re-Analyzed When Design Units They Reference Are Changed in Library.

Compile (UI)



Highlight One Or Multiple Files & Click **Compile**

5 ⇒ Load Design

- UI) *Design -> Load New Design*
- COM) *vsim <top_level_design_unit>*
- VHDL
 - *vsim top_entity top_architecture*
 - Simulates Entity/Architecture Pair
 - Can Also Choose A Configuration
- Verilog
 - *vsim top_level1 top_level2*
 - Simulates Multiple Top Level Modules

Load Design (UI)

The screenshot shows the ModelSim ALTERA 5.4e interface with the 'Load Design' dialog box open. The dialog box has tabs for 'Design', 'VHDL', 'Verilog', 'Libraries', and 'SDF'. The 'Libraries' tab is active, showing a list of libraries under the 'work' library. The 'filter' library is selected. The 'Simulator Resolution' is set to 'ns'. The 'Load' button is highlighted.

Select Library

Select Top-level Module or Entity/Architecture

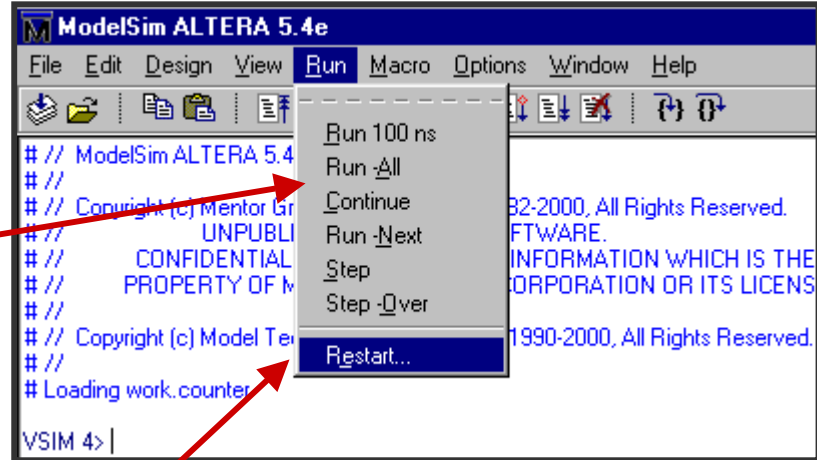
Choose Simulator Resolution

6 ⇒ Start Simulator

- UI) *Run*
- COM) *run* <time_step> <time_units>
- Advances Simulator Amount of Timesteps Specified

Start Simulator (UI)

Choose Number of Timesteps to Advance Simulator



Restart - Reloads Any Design Elements that Have Been Edited & Resets Simulation Time to Zero
COM) **restart**



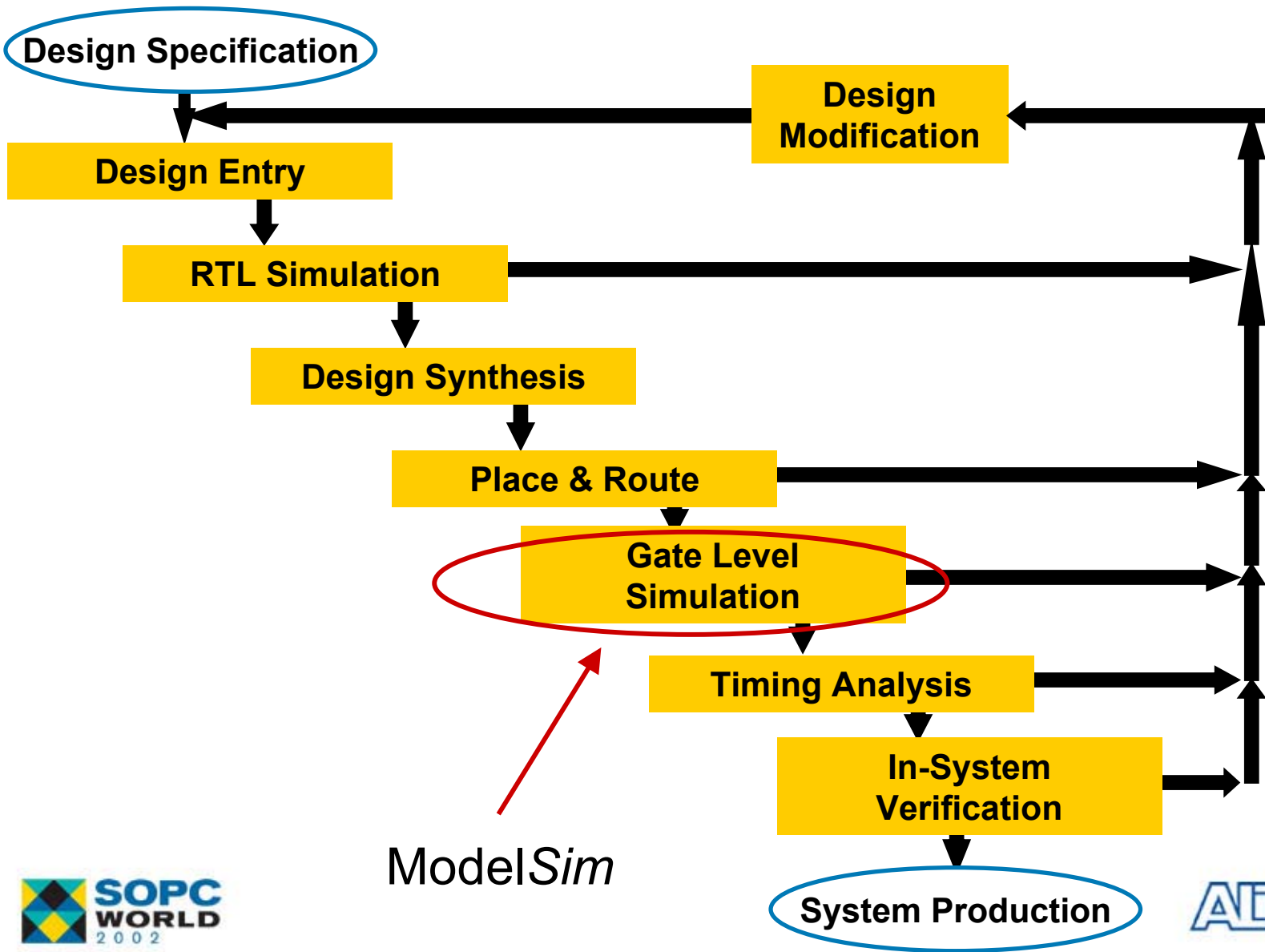
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Simulating with ModelSim Timing Simulation



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Typical PLD Flow



Timing Simulation Files

- Compile Design in Quartus II to Produce Output Files
- Output Simulation Files from Quartus II
 - .VO - Verilog Output File (ATOM)
 - .VHO - VHDL Output File (ATOM)
 - .SDO - Standard Delay Format (SDF) Output File
 - Annotates the delay for the elements in the output files

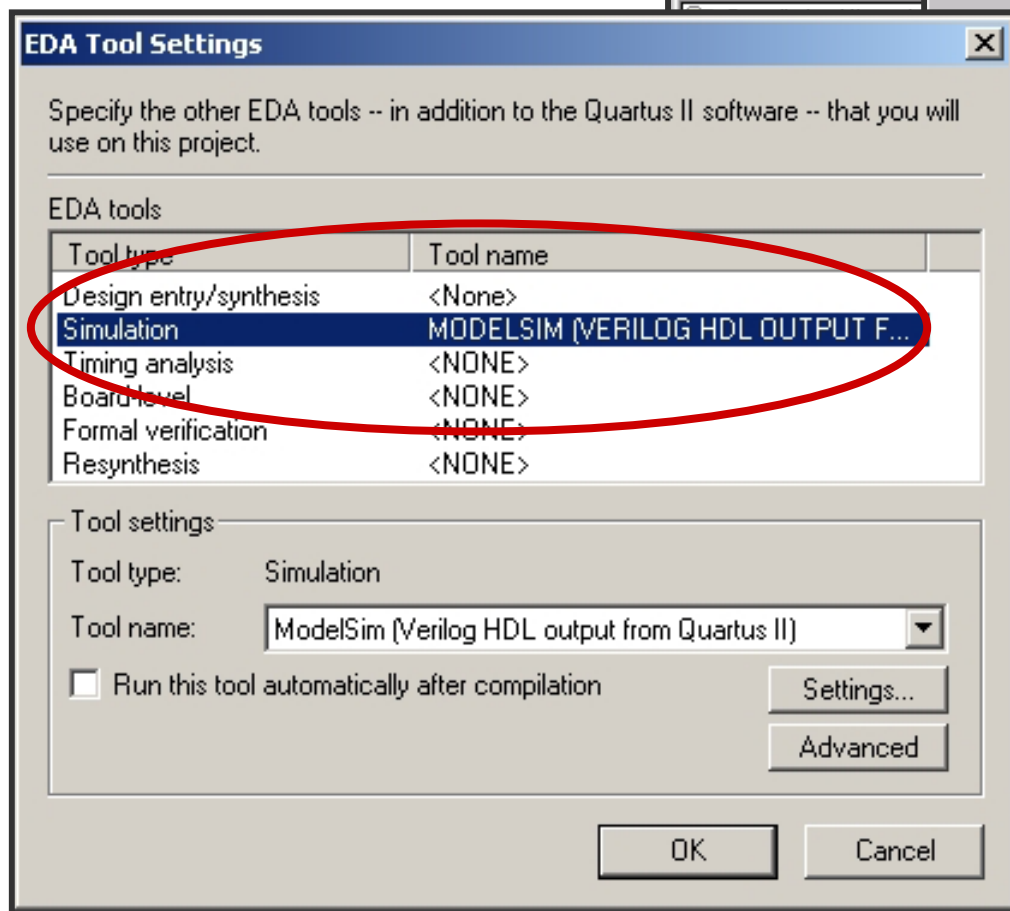
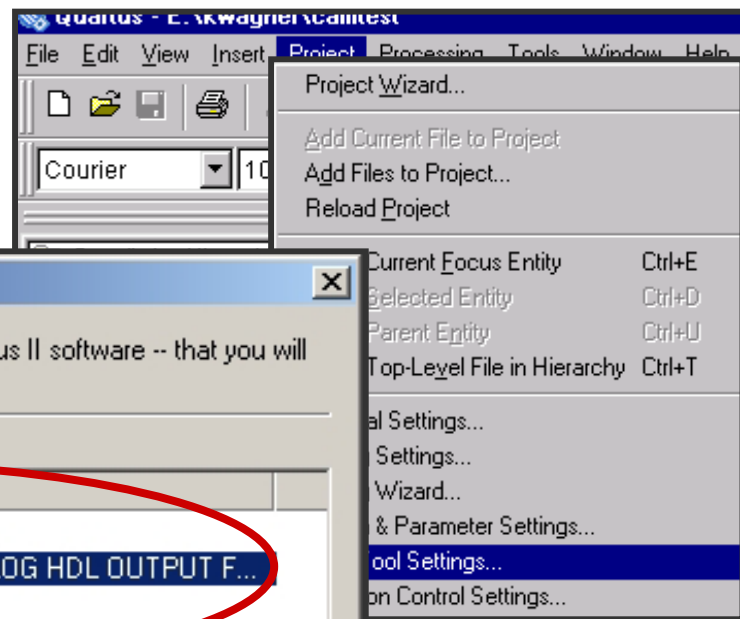


Performing Timing Simulation

- 1) EDA Tool Settings to ModelSim Verilog or VHDL
- 2) Compile Design In Quartus II to Produce Output Files
- 3) Create Testbench / Stimulus
 - Can Use Stimulus from RTL Simulation
- 4) Perform Basic Simulation Steps
 - Compile Quartus II Output File
 - Map To ATOM Libraries
 - Include SDO (Output SDF File) When Loading Design

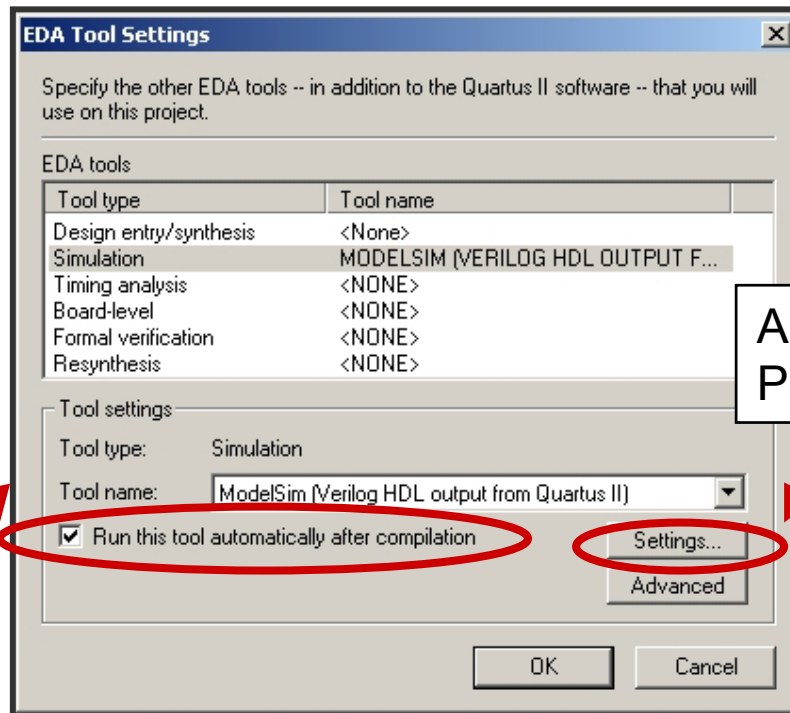
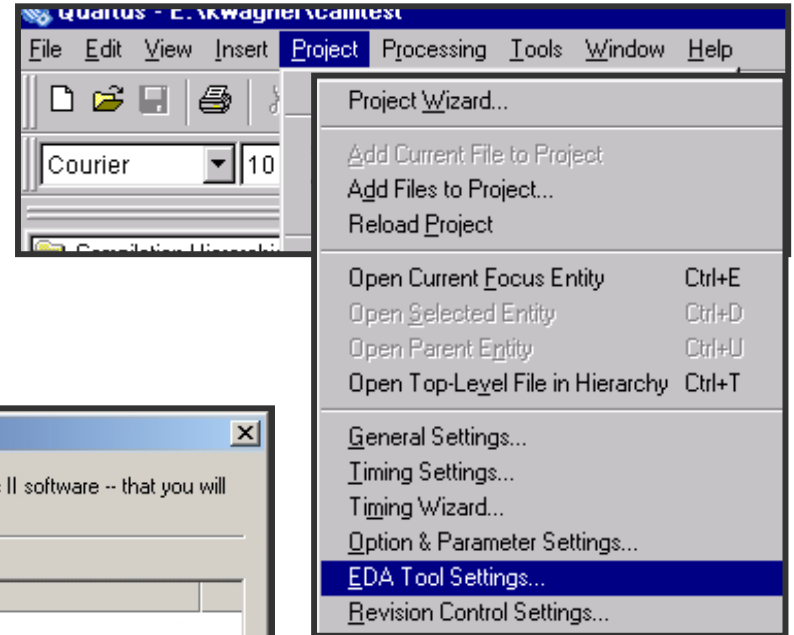
Before Compilation

*Project Menu ->
EDA Tool Settings*



NativeLink

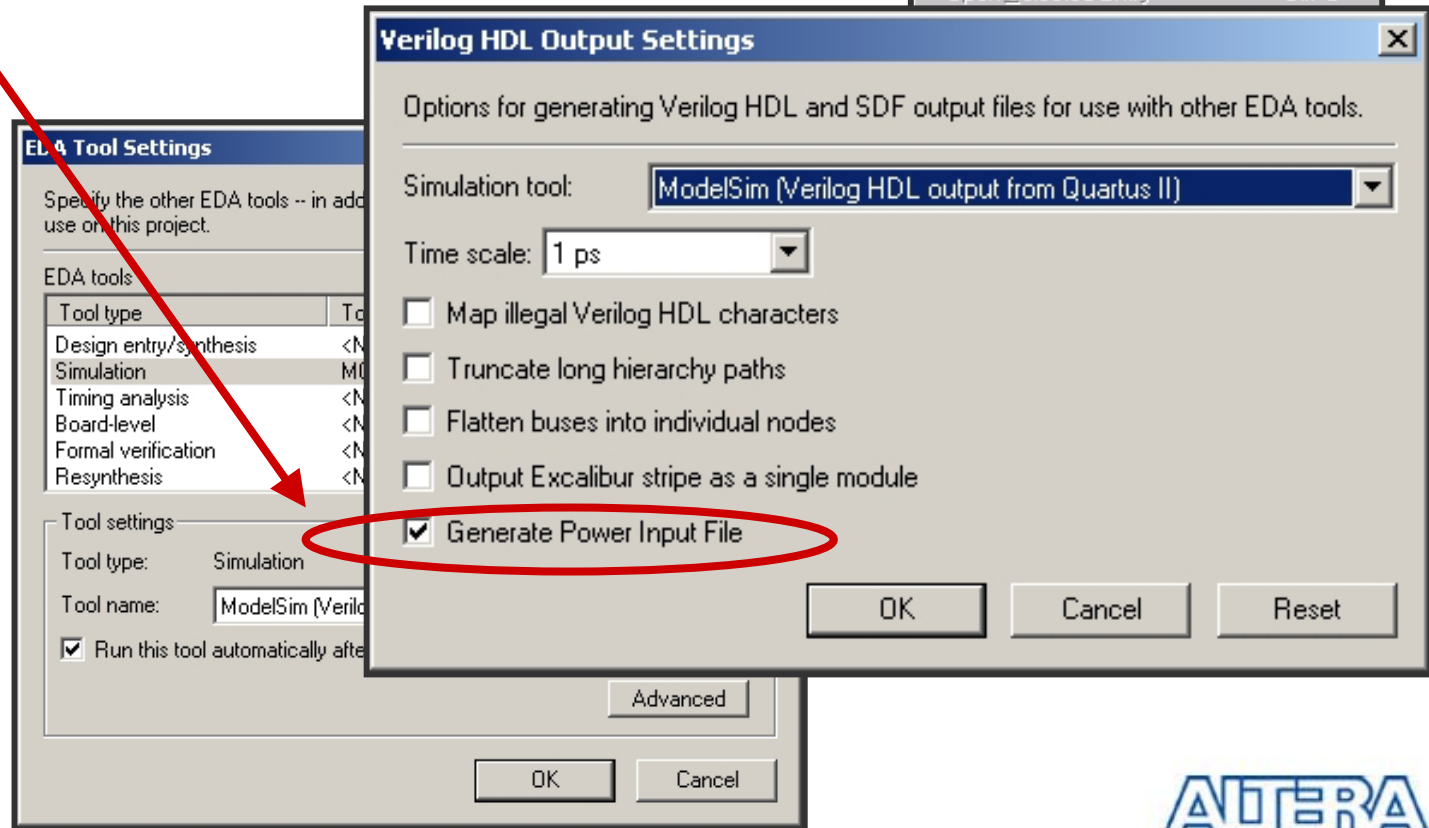
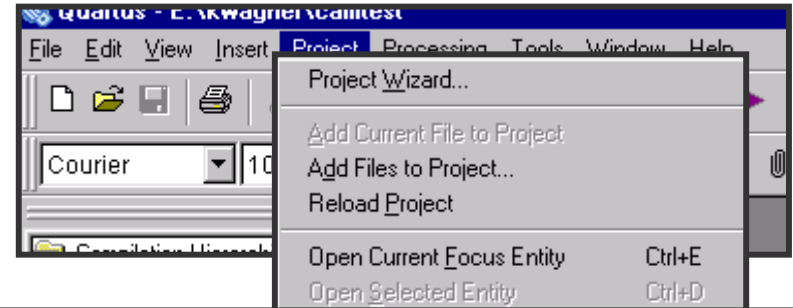
Automatically Starts ModelSim & Compiles the Quartus II Output File after Compilation Is Finished



Additional Settings:
PowerGauge Options

PowerGauge Options for ModelSim

Turn on Generate Power Input File (*.pwr) option



Libraries for Timing Simulation

- *ModelSim* Altera OEM
 - Must use Pre-compiled libraries
Modeltech_ae\altera\vhdl
- *ModelSim* SE/PE
 - ATOM libraries were located at
Quartus\eda\sim_lib
 - Ex) For APEX20KE
 - Verilog : apex20ke_atoms.v
 - VHDL : apex20ke_atoms.vhd &

apex20ke_components.vhd

SDF Annotation

ModelSim ALTERA 5.5a

File Edit Design View Project Run Macro Options Window Help

Load Design

Design VHDL Verilog Libraries **SDF**

Library: work

Simulate

SDF Files

Region/File	Delay
-------------	-------

Add... Delete Edit...

SDF Options

Disable SDF warnings

Reduce SDF errors to warnings

Multi-Source del

latest

min

max

Load Exit Save... Cancel

Click on **SDF Tab** to assign timing file

Click Add button

Multi-source Delay:
Controls How Multiple
Port of Interconnect
Constructs that Terminate
At The Same Port Are
Handled



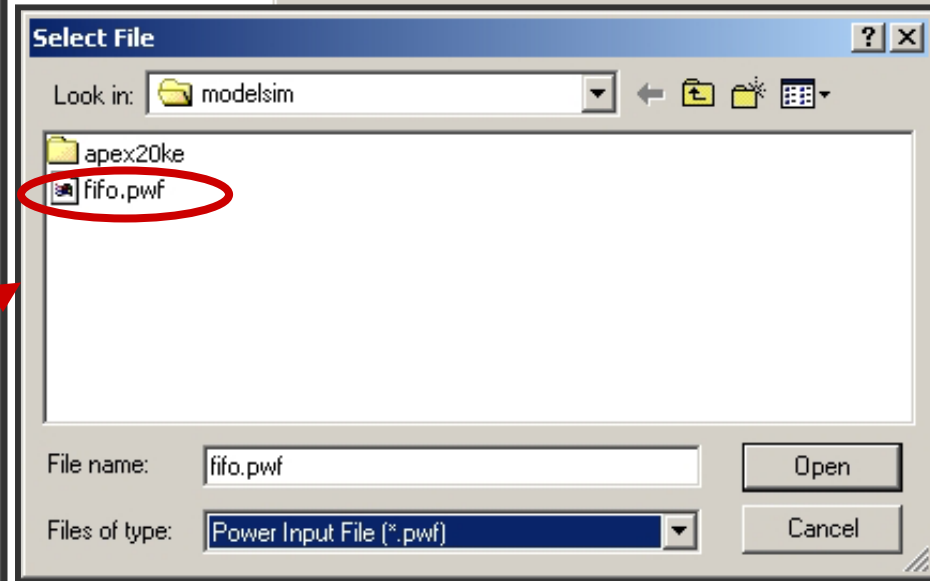
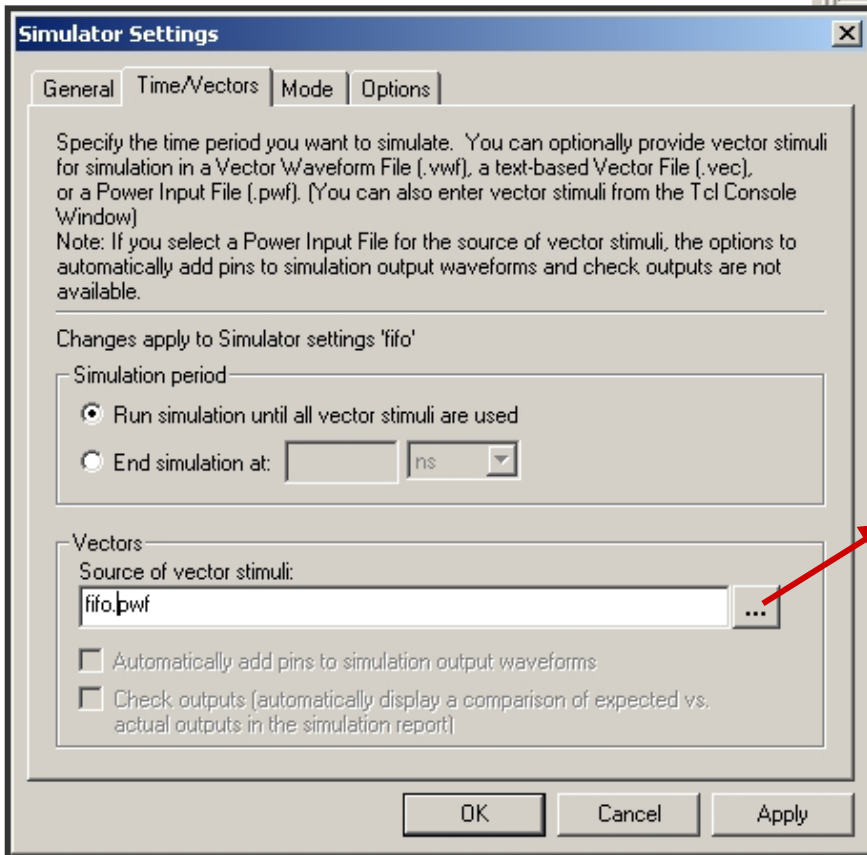
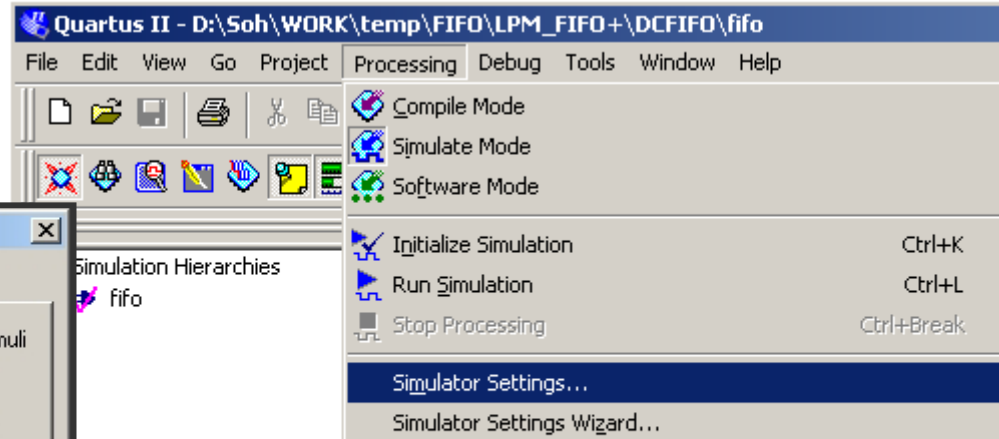
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Calculate Power in Quartus II



Open Power Input File

*Project Menu ->
Simulator Settings*



Running Simulation with PWF

- Select **Run Simulation** from Processing Menu

The screenshot displays the Quartus II interface. On the left, the 'Processing' menu is open, with 'Run Simulation' (Ctrl+L) highlighted. The menu items include: Compile Mode, Simulate Mode, Software Mode, Initialize Simulation (Ctrl+K), Run Simulation (Ctrl+L), Stop Processing (Ctrl+Break), Simulator Settings..., Simulator Settings Wizard..., Set Simulation Focus to Current Entity (Ctrl+J), Add Current Entity at Top Level & Get Focus (Ctrl+Shift+J), Open Simulation Report (Ctrl+R), Open Last Compilation Floorplan, Open Current Assignments Floorplan, Back-Annotate Assignments..., Demote Assignments..., Open Last Simulation Vector Outputs, Open Current Vector Inputs, Overwrite Vector Inputs with Simulation Outputs, Purge Simulator Results from Database, and Open Programmer.

On the right, the 'Simulation Waveform' window is shown for a component named 'filter'. The Master Time Bar is set to 12.125 ns, with a Pointer of 150 ps and an Interval of -11.98 ns. The waveform displays several signals at the 12.125 ns mark:

Name	Value at 12.13 ns
filterclk	B 1
filterre...	B 0
filternew	B 0
filterx	U 16
filtery	B 00000...
filterst...	B idle
lyvalid	B 0
lnext	B 0

Power Report in Quartus II

The screenshot displays the Quartus II interface with the 'fifo Simulation Report' open. The report is divided into a tree view on the left and a summary table on the right. The summary table lists various simulation options and their settings. The 'Total Power' row is circled in red, indicating the power consumption of the design.

Summary		
Option	Setting	
1	Simulation Start Time	0 ps
2	Simulation End Time	95.34 ns
3	Simulation Coverage	27.23 %
4	Number of transitions	279
5	Internal Power	268.89 mW
6	I/O Power	59.97 mW
7	Total Power	328.86 mW

Below the summary table, a progress table shows the status of various modules:

Module	Progress %	Time
Processing Total	100 %	00:00:48
Initialization	100 %	00:00:00
Compiler Total	100 %	00:00:41
Database Builder	100 %	00:00:07
Logic Synthesizer	100 %	00:00:02
Fitter	100 %	00:00:27
Assembler	100 %	00:00:02
Delay Annotator	100 %	00:00:01
Timing Analyzer	100 %	00:00:00
Netlist Writer	100 %	00:00:01
Simulator Total	100 %	00:00:06
Netlist Builder	100 %	00:00:04
Simulator	100 %	00:00:02