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PowerGauge with ModelSim

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Agenda

- Power Estimation in Altera PLD
- PowerGauge™ Power Analysis in Quartus® II Software
- Quartus™ II Software/ Model*Sim* Overview
- Simulating with Model*Sim*
  - Timing Simulation
- Calculate Power in Quartus II Software

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Power Estimation in Altera PLD

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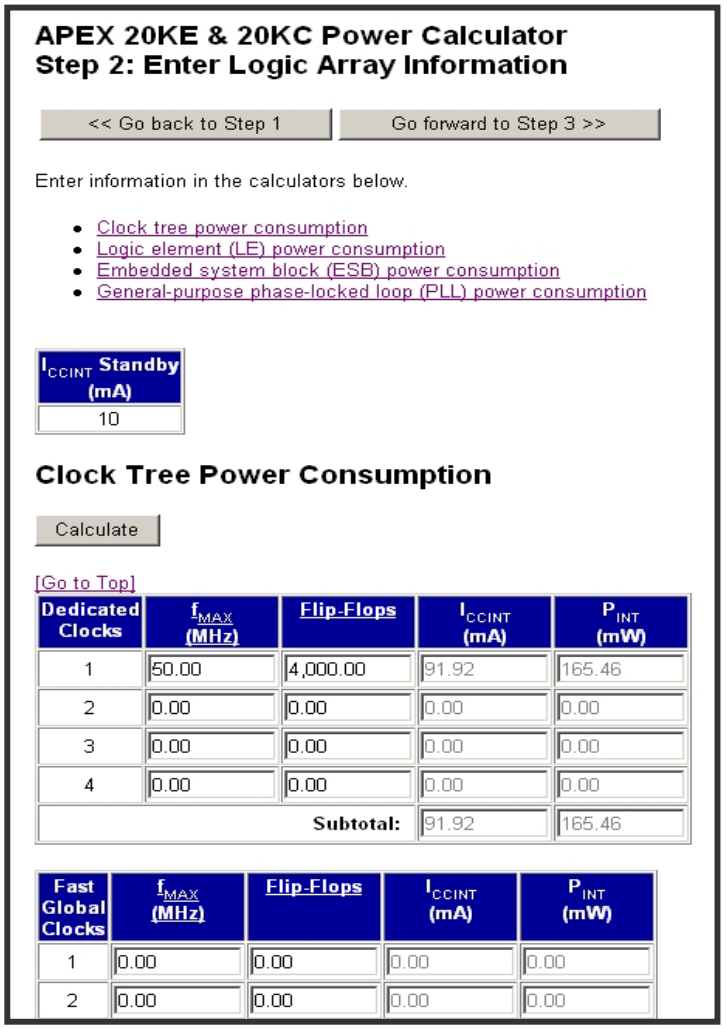
Web-Based Power Calculator

- Easy to Use with Click
- Need to Input Value from Report After Compilation In Quartus II
- Support APEX 20KE/C & APEX™ II & Mercury™ Devices (Supporting Stratix™ Devices Soon)



APEX 20KE & 20KC Power Calculator
Step 2: Enter Logic Array Information

<< Go back to Step 1 | Go forward to Step 3 >>

Enter information in the calculators below.

- Clock tree power consumption
- Logic element (LE) power consumption
- Embedded system block (ESB) power consumption
- General-purpose phase-locked loop (PLL) power consumption

I_{CCINT} Standby (mA)
10

Clock Tree Power Consumption

Calculate

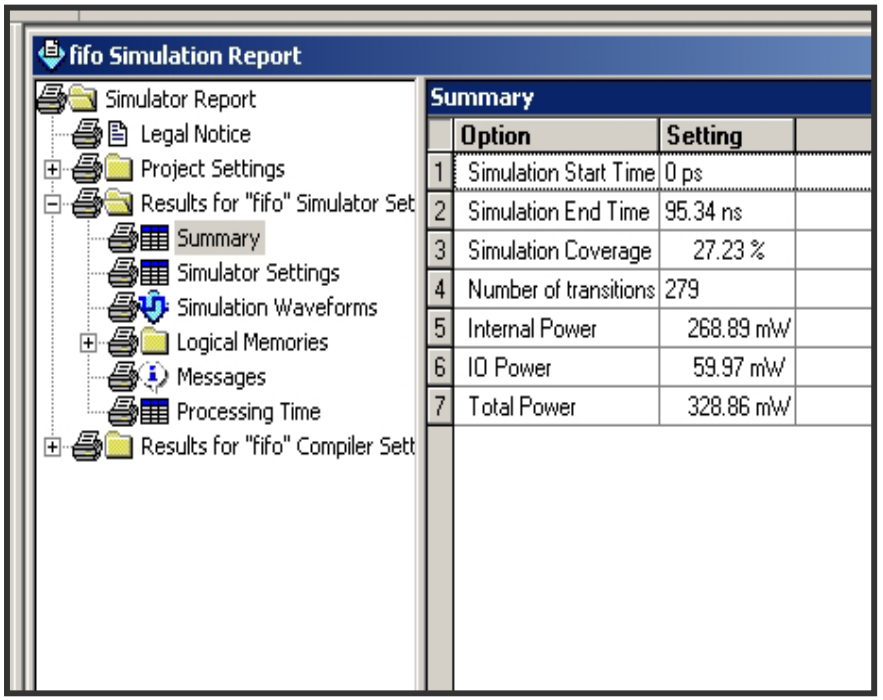
[Go to Top]

Dedicated Clocks	f_{MAX} (MHz)	Flip-Flops	I_{CCINT} (mA)	P_{INT} (mW)
1	50.00	4,000.00	91.92	165.46
2	0.00	0.00	0.00	0.00
3	0.00	0.00	0.00	0.00
4	0.00	0.00	0.00	0.00
		Subtotal:	91.92	165.46

Fast Global Clocks	f_{MAX} (MHz)	Flip-Flops	I_{CCINT} (mA)	P_{INT} (mW)
1	0.00	0.00	0.00	0.00
2	0.00	0.00	0.00	0.00

Quartus II Power Calculator

- 1. Must Make Vector Wave Form File (*.vwf) for Using PowerGauge in Quartus II Software
- 2. More Accurate than Web Based Power Calculator
- 3. Support APEX Family & Mercury Devices (Supporting Stratix Devices in Next Version)



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PowerGauge in Quartus II

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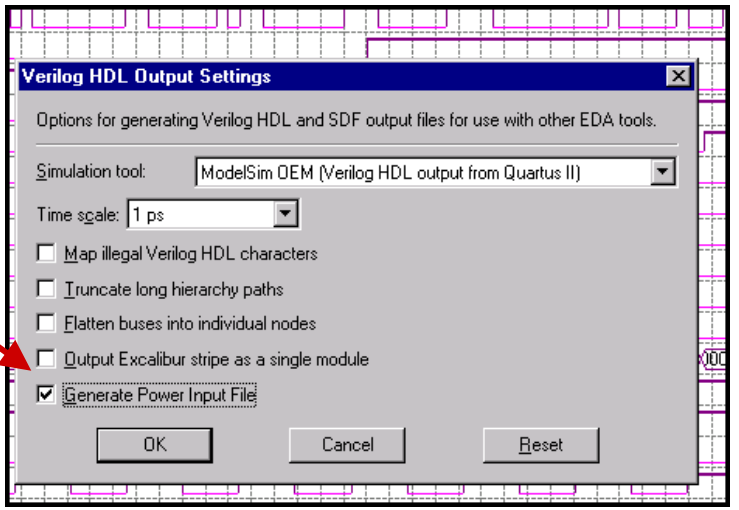
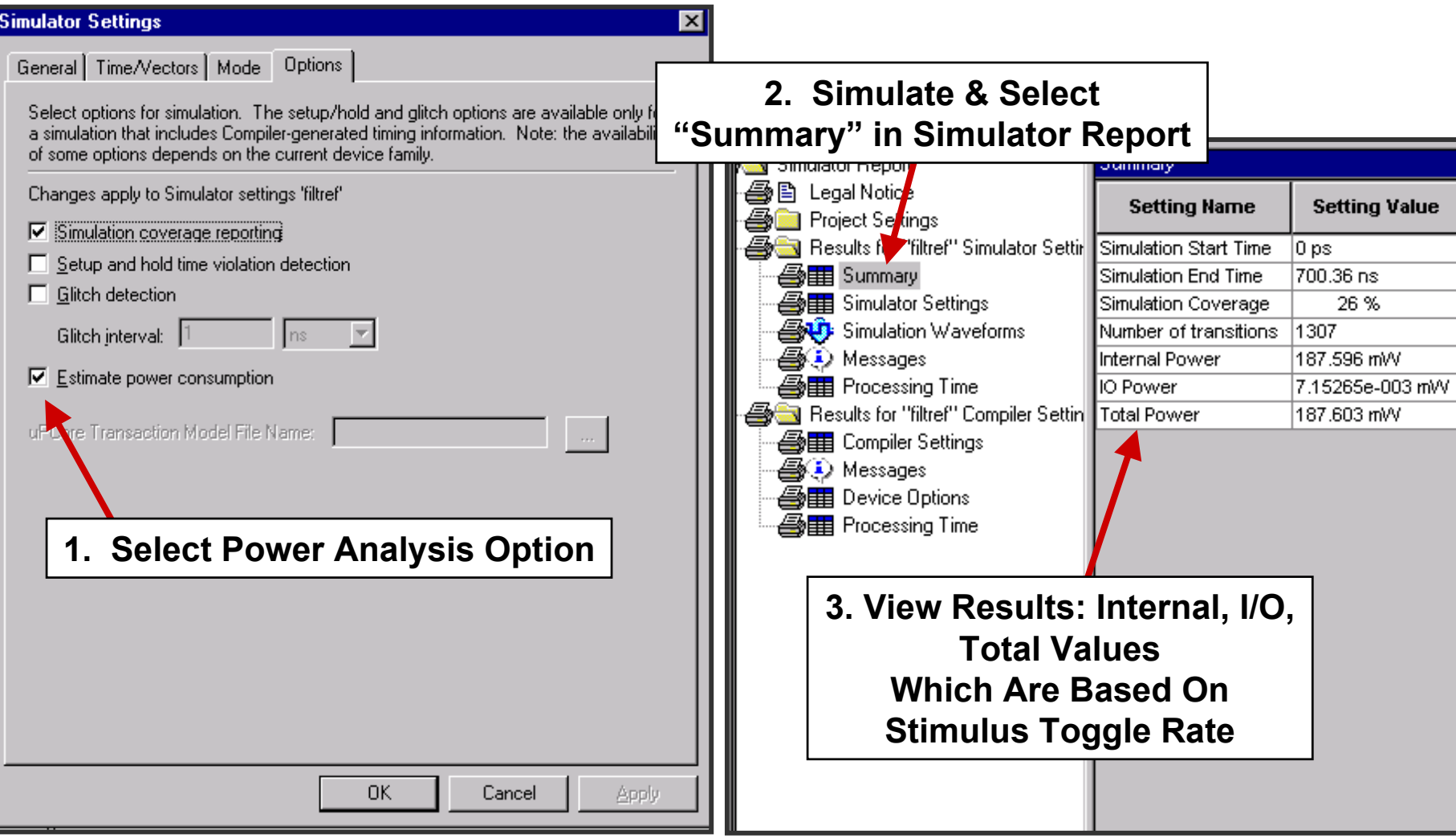
PowerGauge Analysis Software

- Estimates Power Consumption Based on Toggle Rate
  - Toggle Rate Derived from User Generated Simulation Vectors
  - Use Quartus II Simulator
- Provides Support For Multiple I/O Standards
- Supports APEX 20KE & Mercury Families
- Modelsim Can Output .Pwf File That Can Be Read by the Quartus II Simulator

Project >EDA Tool Settings >Modelsim Settings Generate Power Input File



Power Analysis in Quartus II



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Quartus II/ Model*Sim* Overview

QUARTUS™ II

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Basic Simulation Steps

1 ⇨ Change Directory

2 ⇨ Create Library(s)

3 ⇨ Map Library to Physical Directory

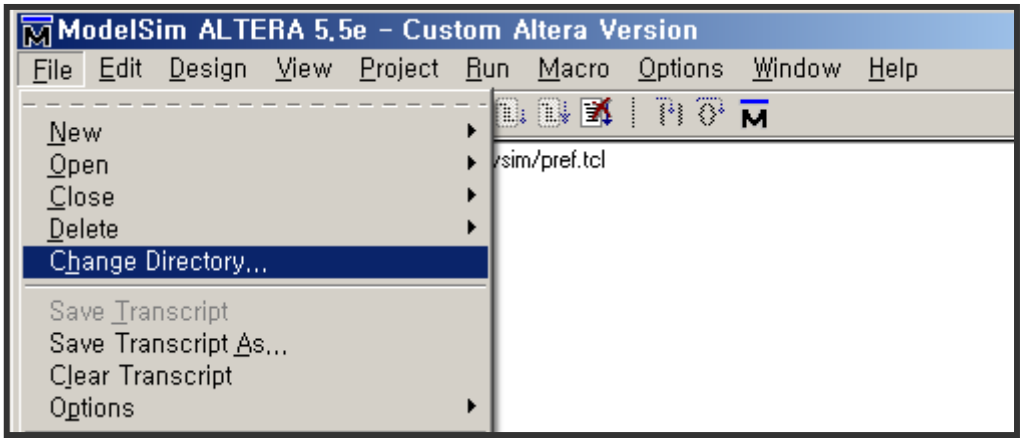
4 ⇨ Compile Source Code

- All HDL Code Must Be Compiled
- Different for Verilog & VHDL

5 ⇨ Load Design

6 ⇨ Start Simulator

1 ⇨ Change Directory



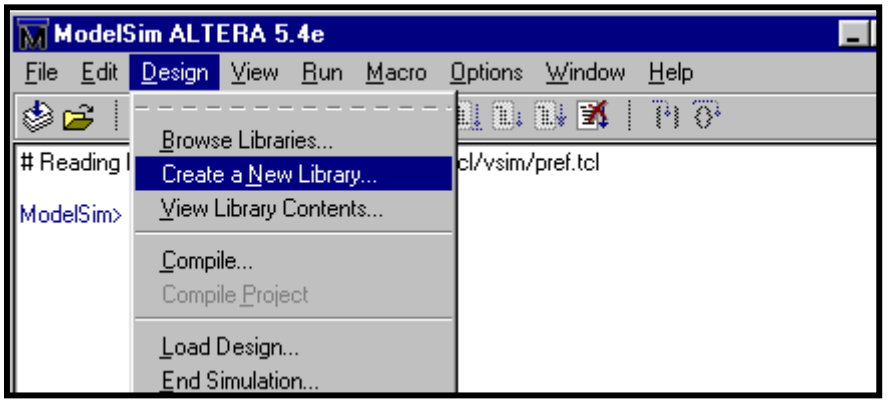
UI) From within Main Window:

File -> Change Directory

Cmd) From within Main, transcript window:

ModelSim> *cd <drive>:/<directory name>*

2 ⇨ Creating ModelSim Library(s)



UI) From within Main Window:

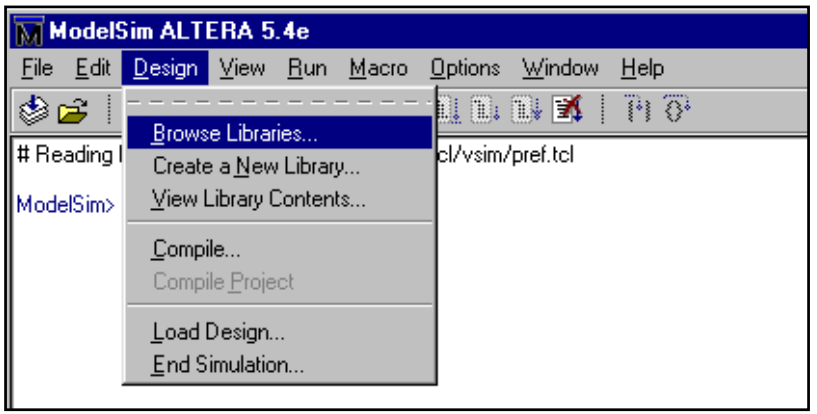
Design -> Create a New Library

Cmd) from within Main, transcript window:

ModelSim> *vlib <library name>*

3 ⇨ Map Logical Library Name(s)

- Syntax: *vmap* <logical_name> <directory_path>



UI) From within Main Window:

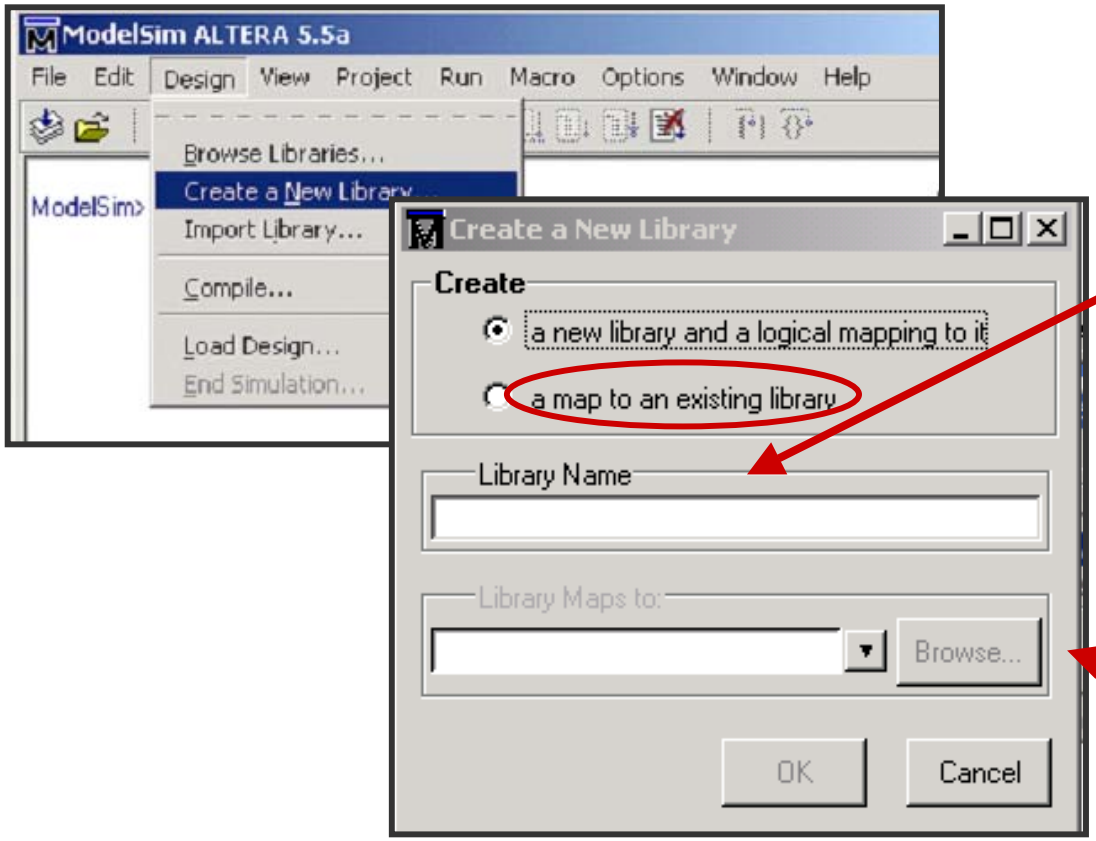
Design -> Browse Libraries

Design -> Create a New Library

Cmd) From within Main, Transcript Window:

ModelSim> *vmap my_work c:\my_design\my_lib*

Mapping Existing Libraries (UI)



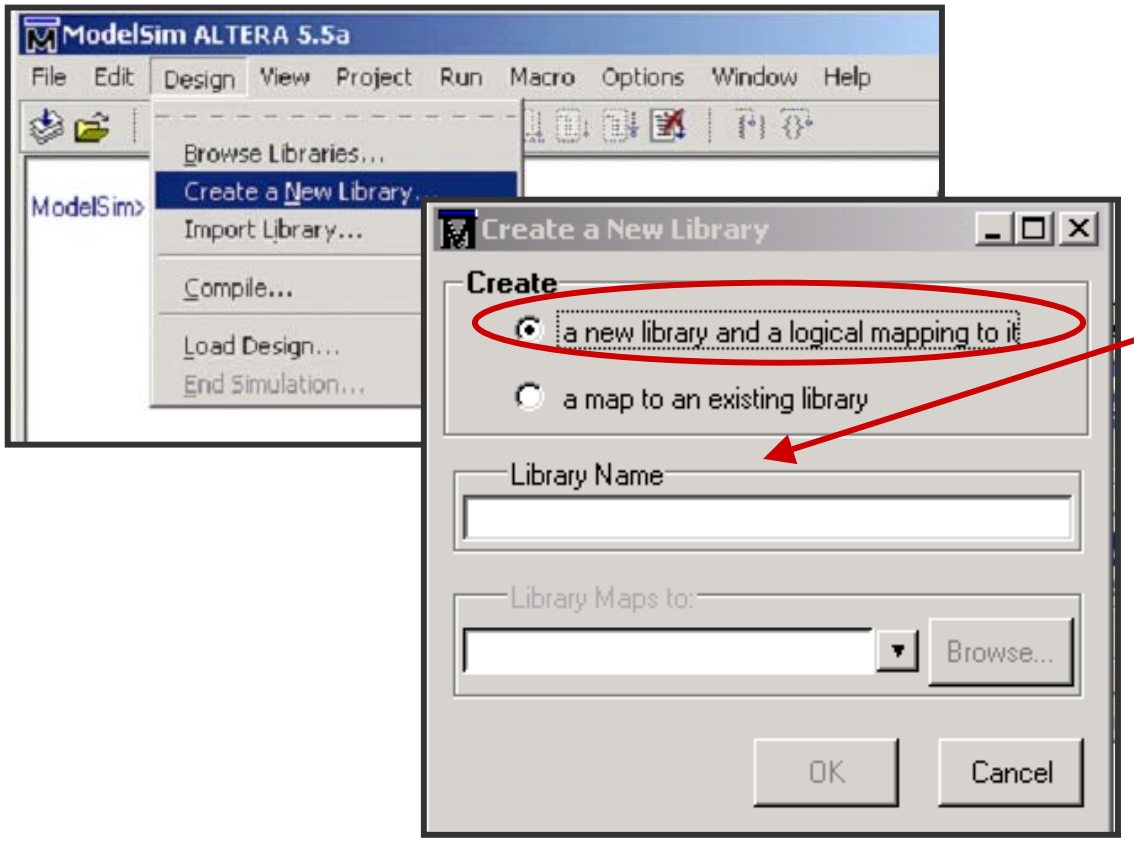
Select *Map To An Existing Library* & Type Library Name

Use This Command To Map to Library Directory of Pre-Compiled Design Units

Browse to Library Directory

-> vmap lpm_sim c:\QuartusII\library\lpm

Mapping Existing Libraries (UI)

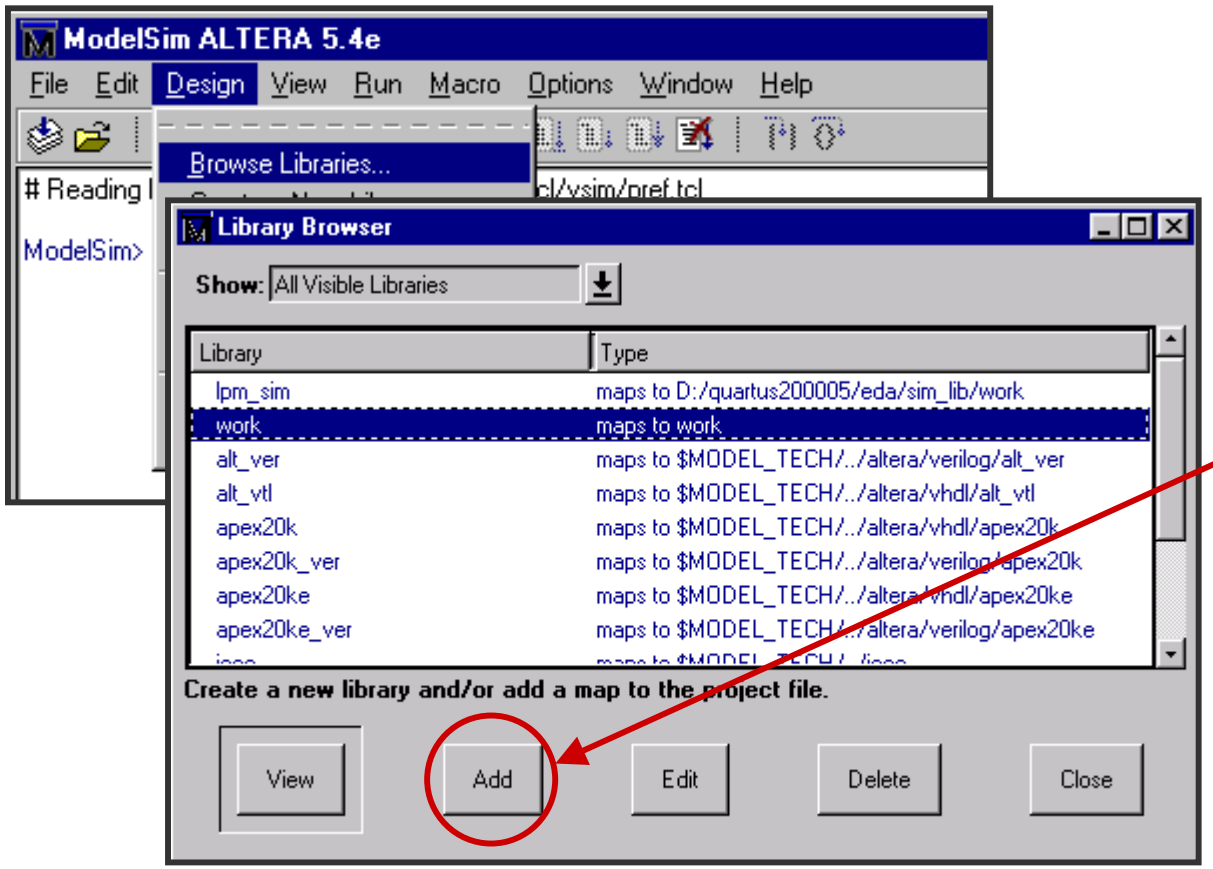


Select A New Library & A Logical Mapping to It & Type Library Name

This Command Creates Library Subdirectory in Local Directory & Then Sets Mapping for It

```
-> vlib my_lib
-> vmap my_lib my_lib
```

Mapping Libraries (UI)



Use Add Button to Create New Library & Map

4 ⇨ Compile Source Code (VHDL)

- UI) ***Design -> Compile***
- Cmd) *vcom* -work <library_name> <*file1*>.vhd <*file2*>.vhd
  - Files Are Compiled in Order They Appear
  - Compilation Order/Dependencies (Next Slide)
- '87 VHDL is default
  - UI) Use Default Options button to set '93
  - Cmd) Use -93 Option (Must Be First Argument)
- Default Compiles into Library Work
  - Ex. *Vcom* -93 my_design.vhd

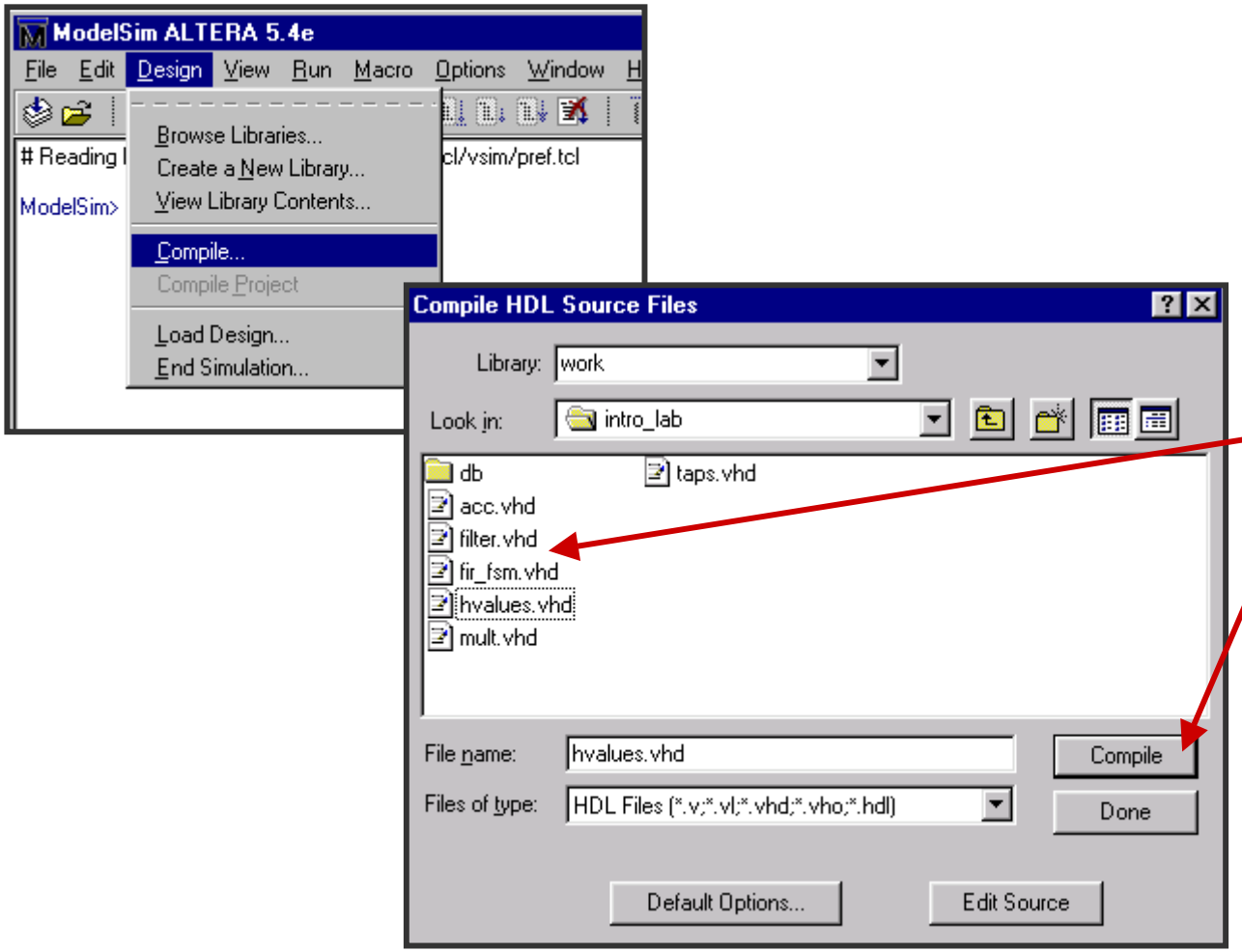
Note: Design Units Must Be Re-Analyzed When Design Units They Reference Are Changed in Library.

4 ⇨ Compile Source Code (Verilog)

- UI) ***Design -> Compile***
- Cmd) *vlog* -work <library_name> <*file1*>.v <*file2*>.v
  - Files Are Compiled In Order They Appear
  - Order Of Files or Compilation Does Not Matter
- Supports Incremental Compilation
- Default Compiles Into Library Work
  - Ex. *vlog* my_design.v

Note: Design Units Must Be Re-Analyzed When Design Units They Reference Are Changed in Library.

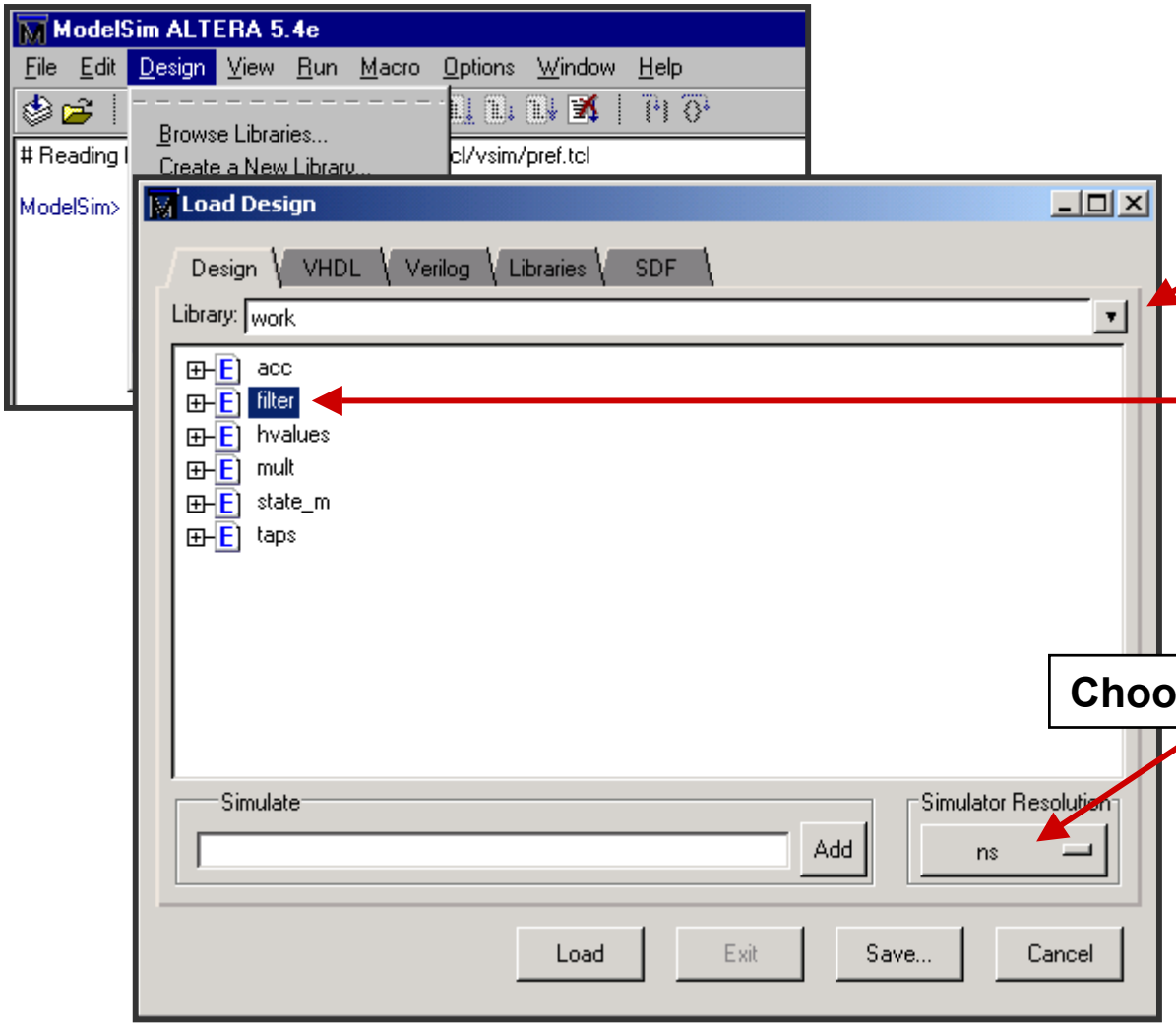
Compile (UI)


ModelSim ALTERA 5.4e
File Edit Design View Run Macro Options Window H
Browse Libraries...
Create a New Library...
View Library Contents...
Compile...
Compile Project
Load Design...
End Simulation...
Reading
cl/vsim/pref.tcl
ModelSim>
Compile HDL Source Files
Library: work
Look in: intro_lab
db
taps.vhd
acc.vhd
filter.vhd
fir_fsm.vhd
hvalues.vhd
mult.vhd
File name: hvalues.vhd
Files of type: HDL Files (*.v;*.vl;*.vhd;*.vho;*.hdl)
Compile
Done
Default Options...
Edit Source
Highlight One Or Multiple Files & Click Compile

5 ⇨ Load Design

- UI) ***Design -> Load New Design***
- COM) *vsim* <top_level_design_unit>
- VHDL
  - *vsim* top_entity top_architecture
    - Simulates Entity/Architecture Pair
    - Can Also Choose A Configuration
- Verilog
  - *vsim* top_level1 top_level2
    - Simulates Multiple Top Level Modules

Load Design (UI)



Select Library

Select Top-level **Module** or **Entity/Architecture**

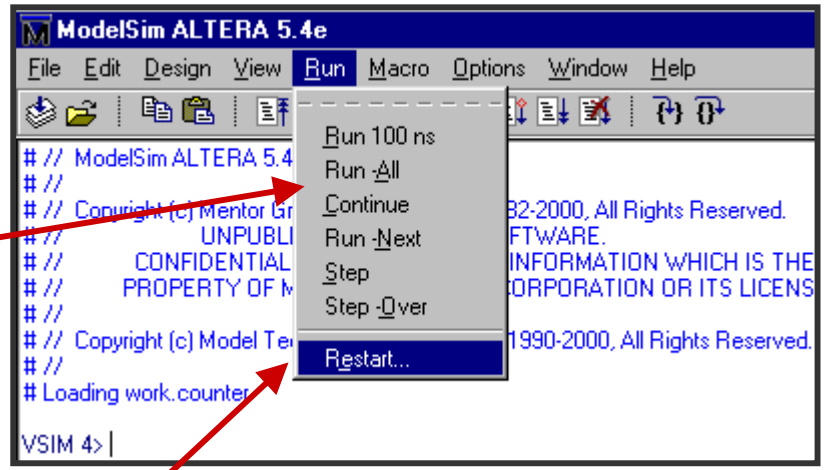
Choose Simulator Resolution

6 ⇨ Start Simulator

- UI) ***Run***
- COM) *run* <time_step> <time_units>
- Advances Simulator Amount of Timesteps Specified

Start Simulator (UI)

Choose Number of Timesteps to Advance Simulator



Restart **- Reloads Any Design Elements that Have Been Edited & Resets Simulation Time to Zero**
COM) **restart**

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Simulating with ModelSim Timing Simulation

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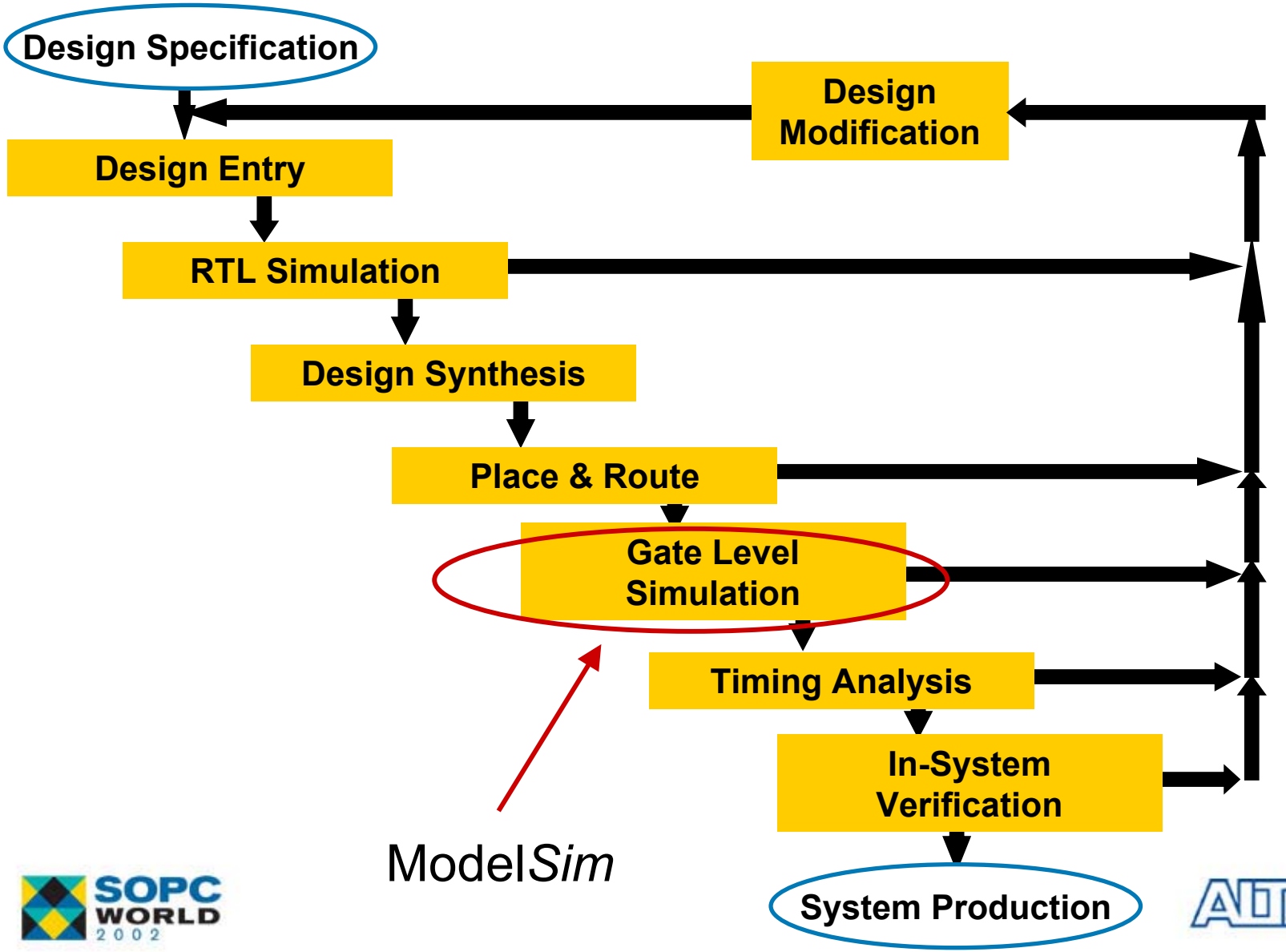
Typical PLD Flow



Timing Simulation Files

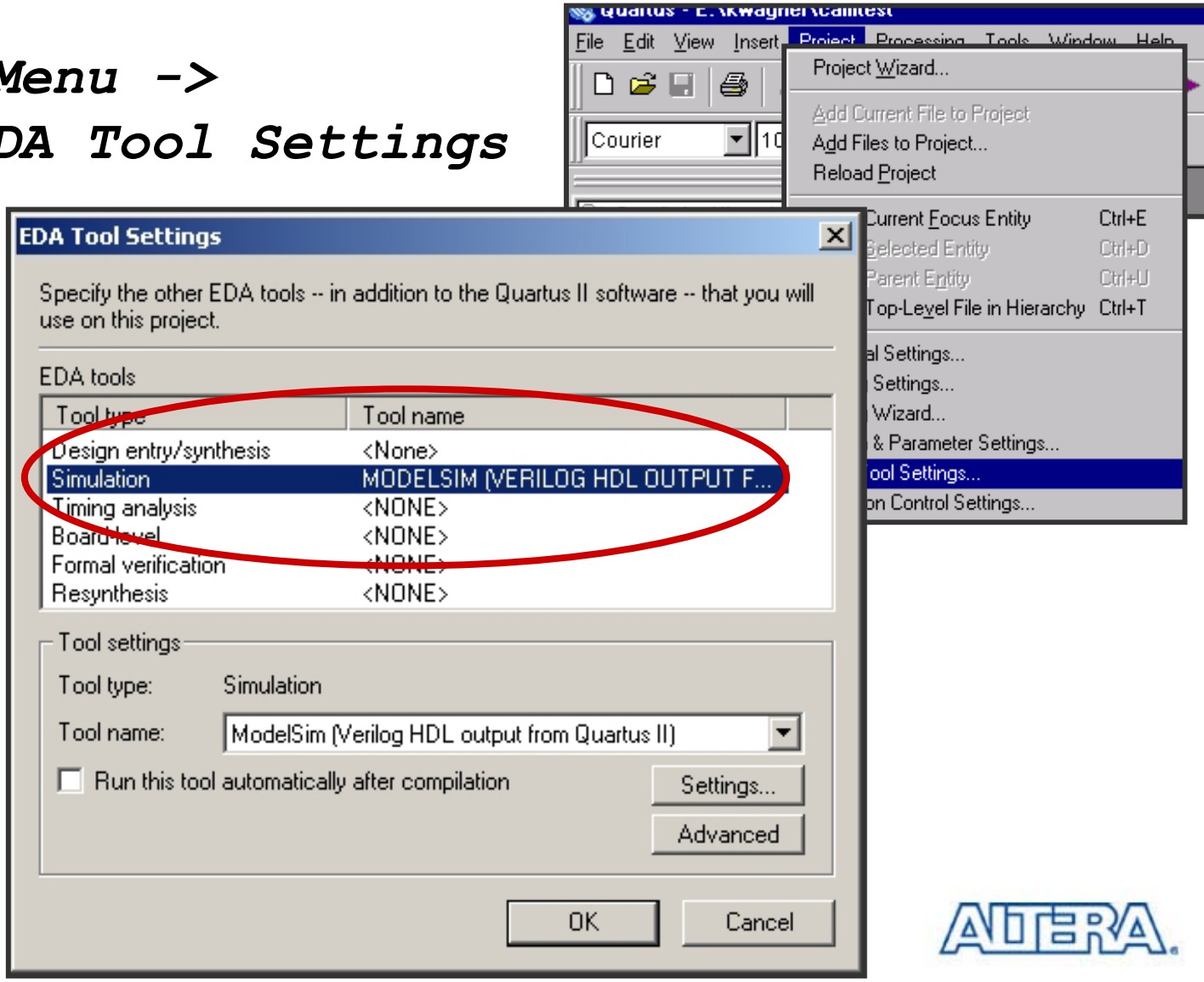
- Compile Design in Quartus II to Produce Output Files
- Output Simulation Files from Quartus II
  - .VO - Verilog Output File (ATOM)
  - .VHO - VHDL Output File (ATOM)
  - .SDO - Standard Delay Format (SDF) Output File
    - Annotates the delay for the elements in the output files

Performing Timing Simulation

1) EDA Tool Settings to Model*Sim* Verilog or VHDL
2) Compile Design In Quartus II to Produce Output Files
3) Create Testbench / Stimulus
   - Can Use Stimulus from RTL Simulation
4) Perform Basic Simulation Steps
   - Compile Quartus II Output File
   - Map To ATOM Libraries
   - Include SDO (Output SDF File) When Loading Design

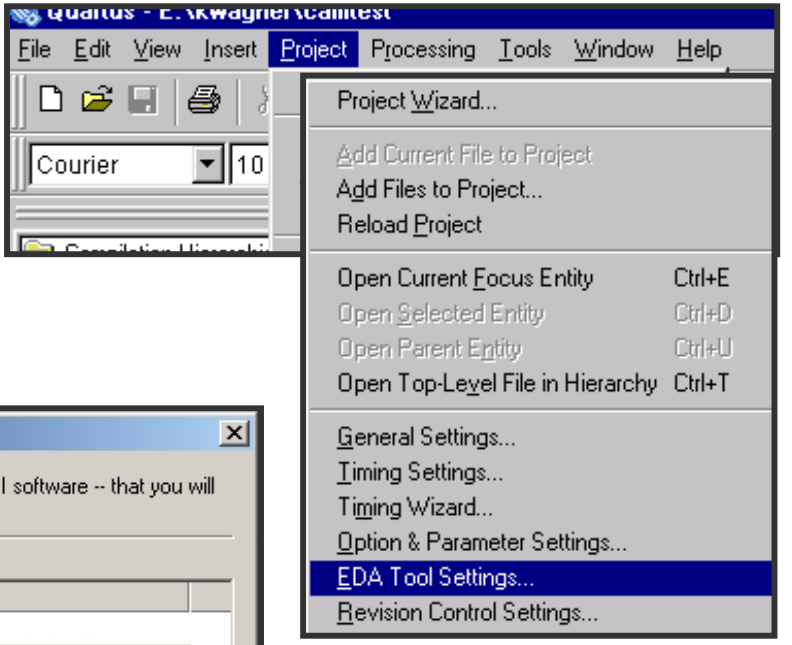
Before Compilation

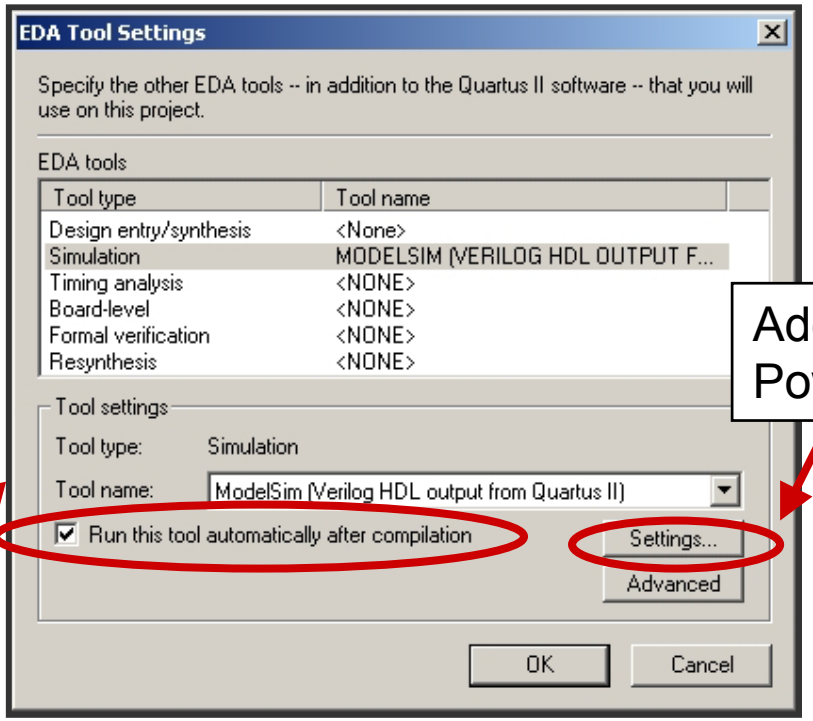
Project Menu ->
EDA Tool Settings



NativeLink

Automatically Starts Model*Sim* & Compiles the Quartus II Output File after Compilation Is Finished

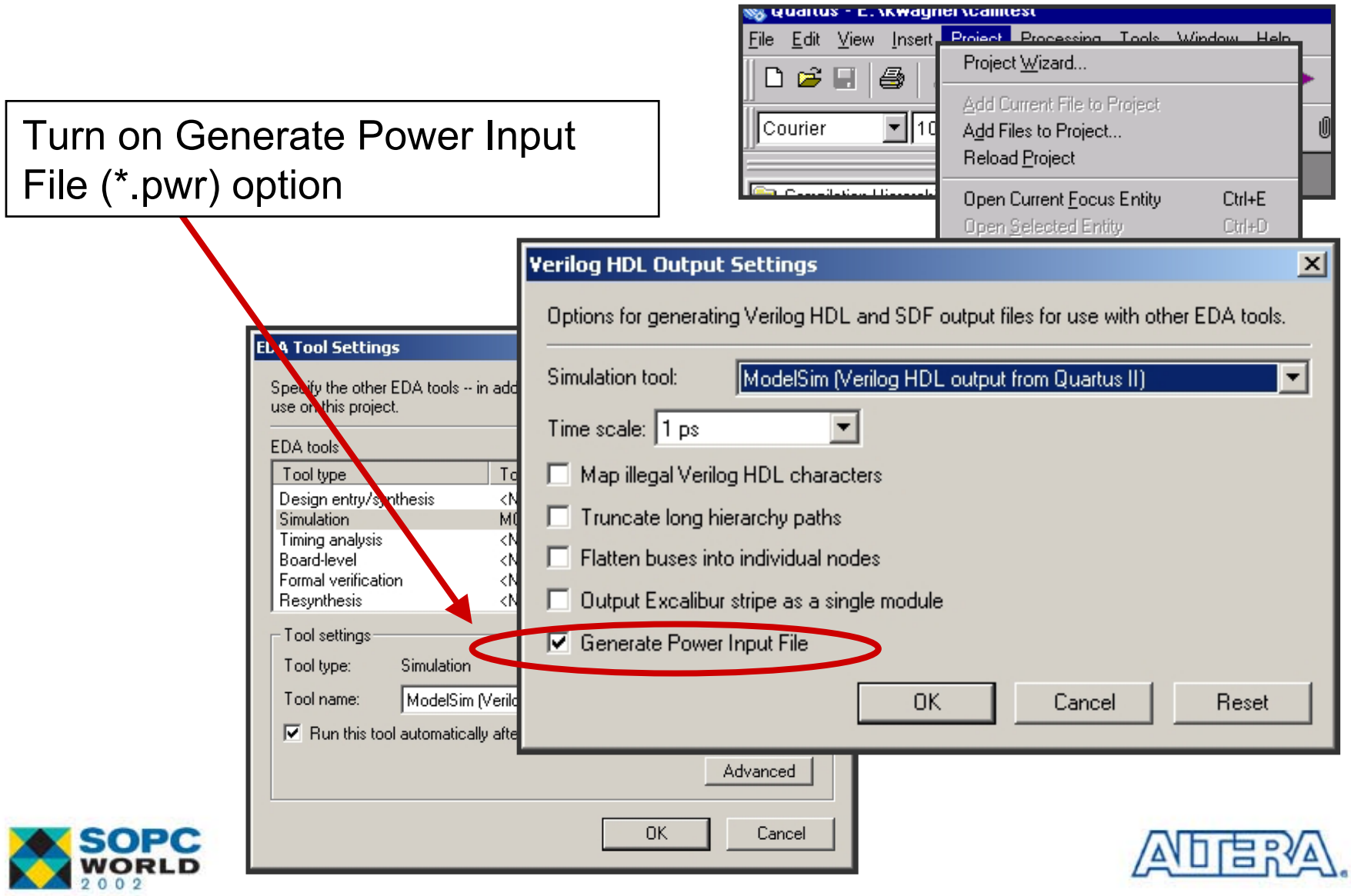




Additional Settings: PowerGauge Options

PowerGauge Options for ModelSim

Turn on Generate Power Input File (*.pwr) option



Libraries for Timing Simulation

- Model*Sim* Altera OEM

  - Must use Pre-compiled libraries
  Modeltech_ae\altera\vhdl

- Model*Sim* SE/PE

  - ATOM libraries were located at
  Quartus\eda\sim_lib

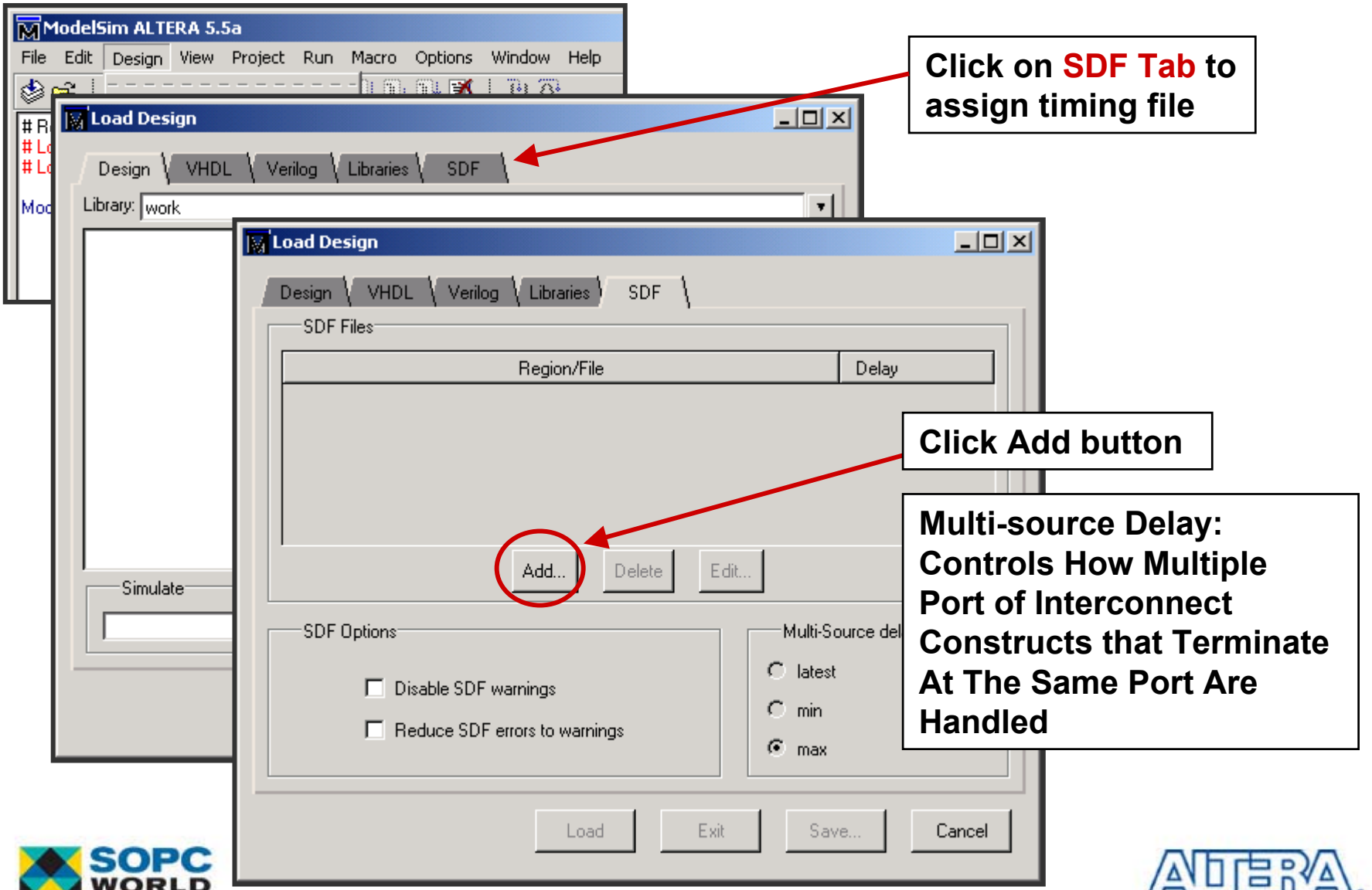
  Ex) For APEX20KE

  Verilog : apex20ke_atoms.v

  VHDL : apex20ke_atoms.vhd &

  apex20ke_components.vhd

SDF Annotation



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Calculate Power in Quartus II

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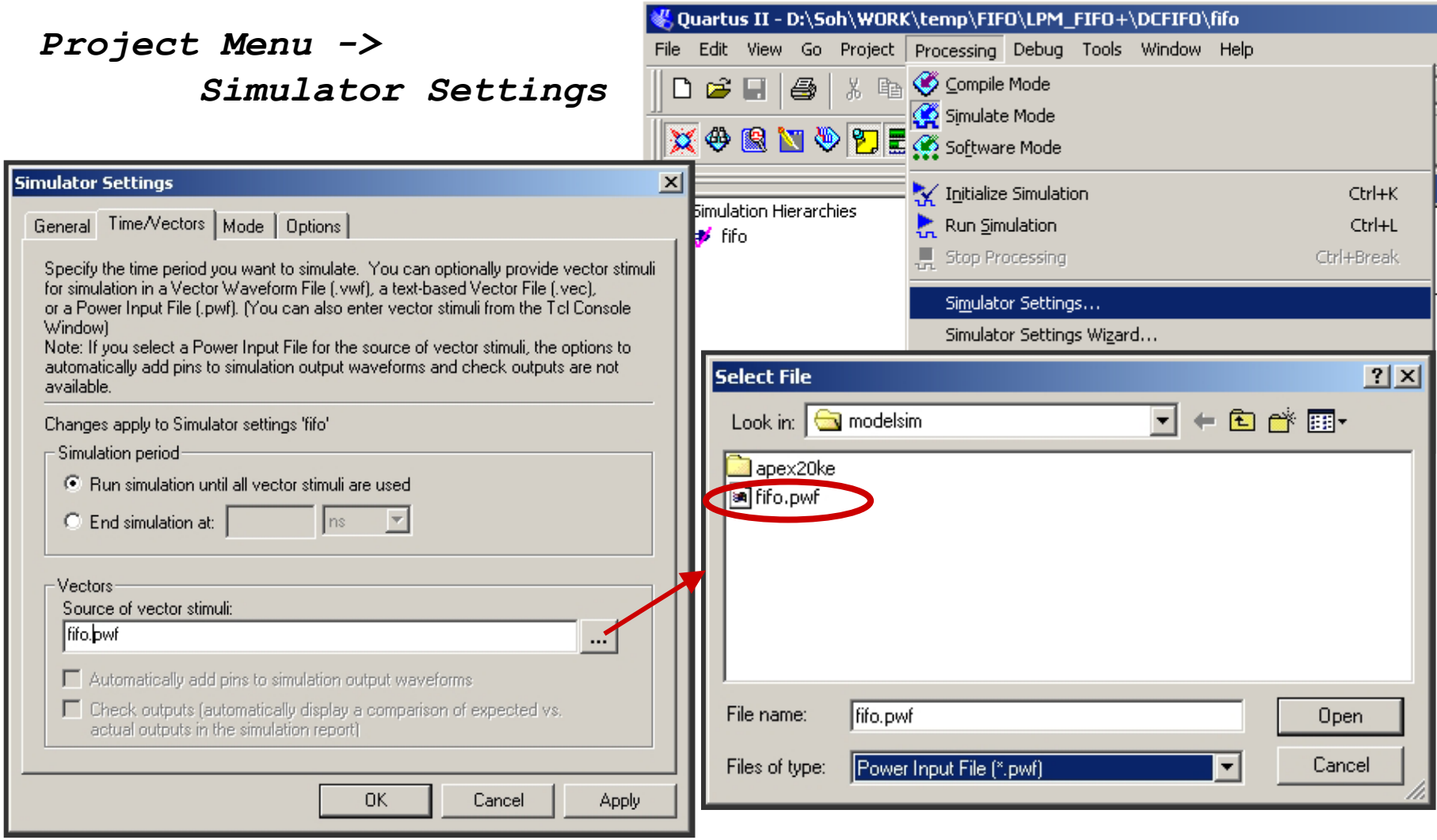
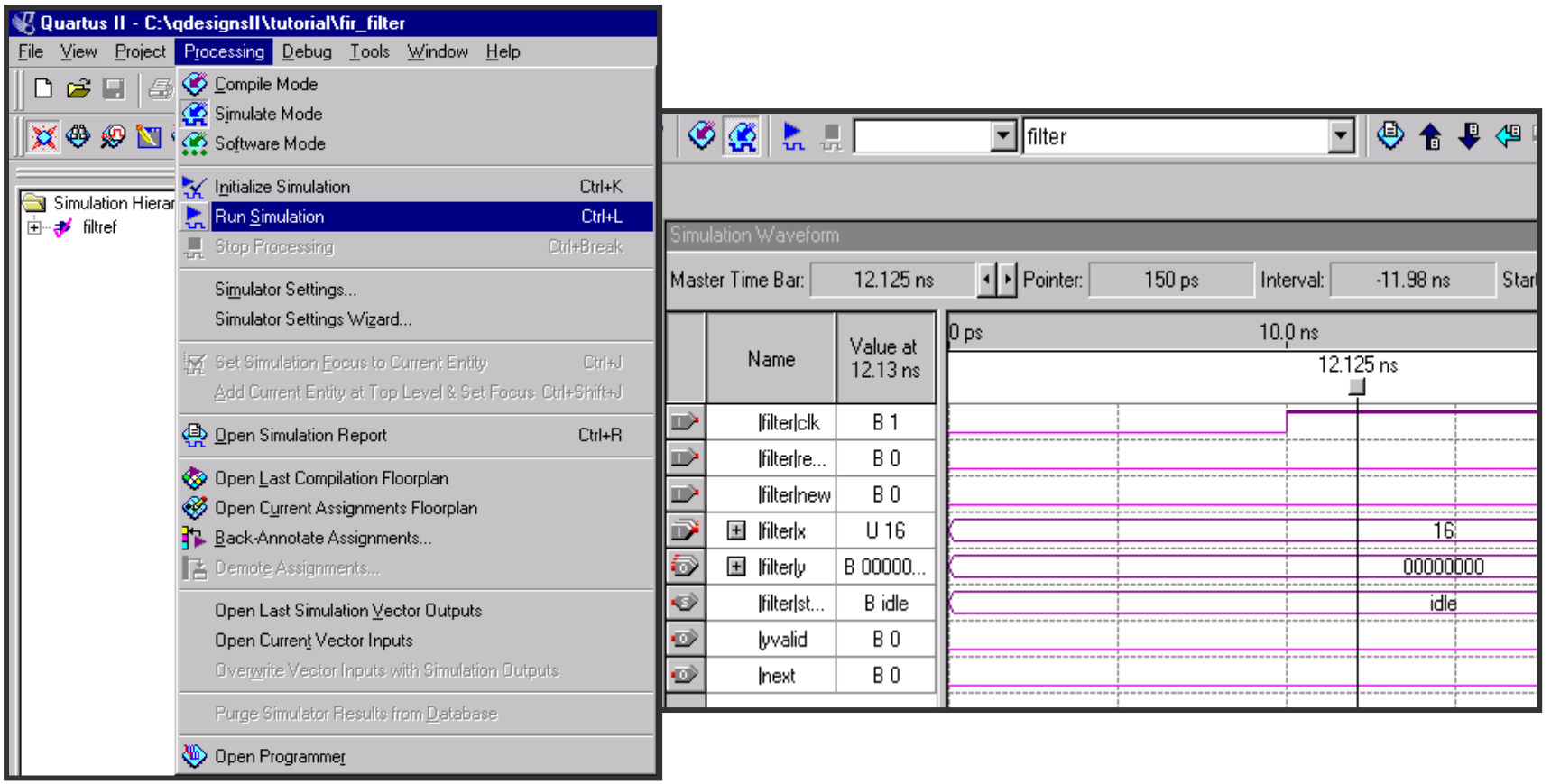
Open Power Input File

Project Menu ->
Simulator Settings



Running Simulation with PWF

- Select **Run Simulation** from Processing Menu



Power Report in Quartus II