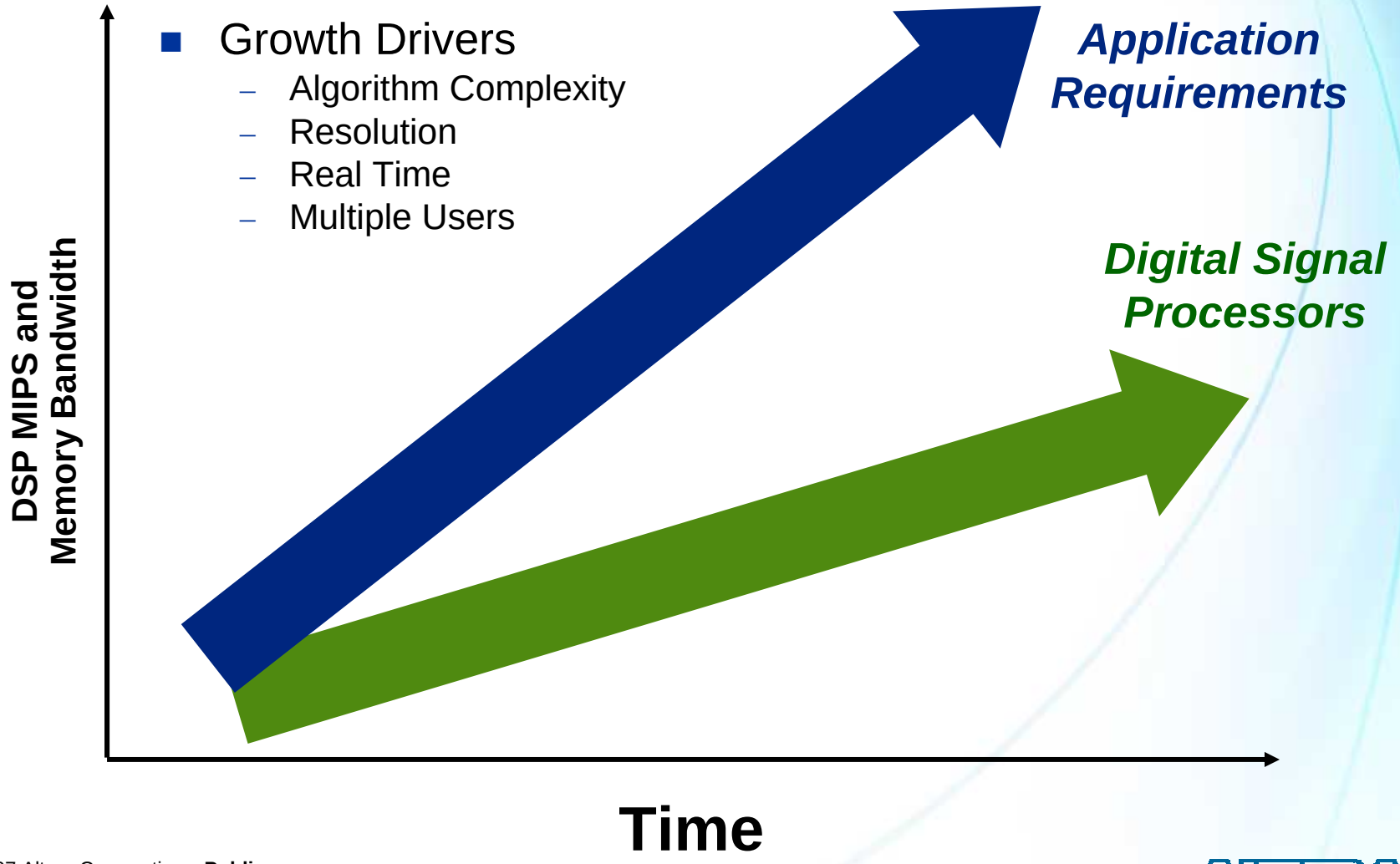
High-Performance Digital Signal Processing (DSP) Applications with Serial RapidIO Standard

Agenda

- High-performance DSP applications
- Serial RapidIO™ review
- Altera® Serial RapidIO solution
- Altera Serial RapidIO demo

Growing Demand for MIPS and Memory Bandwidth



DSP vs. FPGA Comparison – 1

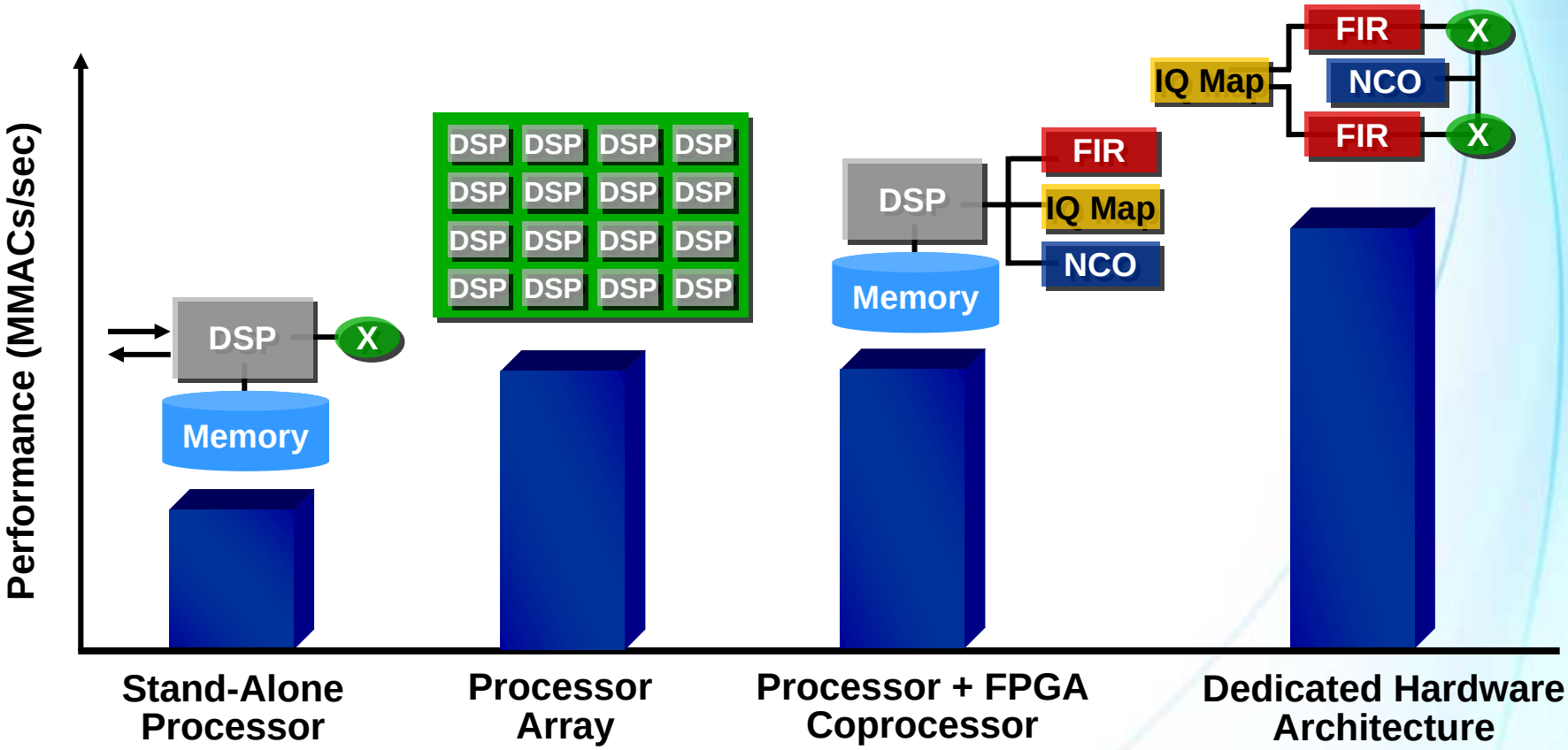
	DSP	FPGA
Advantages	■ High clock rate ■ Rapid software development in C++	■ High number of instructions/clock ■ High number of multipliers ■ High bandwidth flexible I/O and memory connectivity
Disadvantages	■ Limited number of instructions/clock ■ Limited number of multipliers ■ Limited memory and device connectivity	■ Longer development time ■ Typically lower clock rates

DSP vs. FPGA Comparison – 2

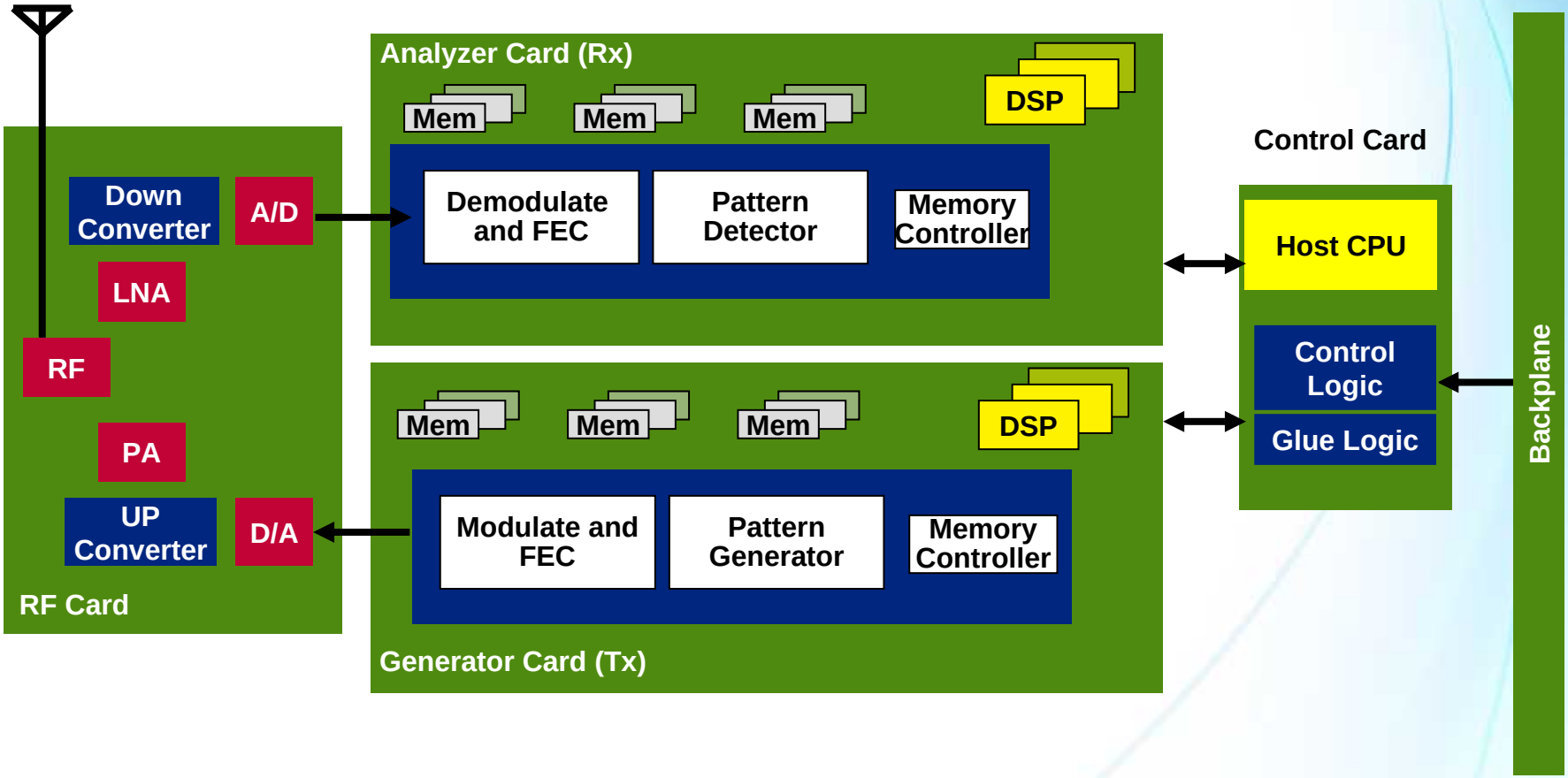
Functions	DSP	FPGA
Maximum clock rate	1 GHz	370 MHz
Maximum number of multipliers	4 (16-bit X16-bit)	Over 700 18-bit X 18-bit (384 HW + 300 LE) or over 1400 9-bit X 9-bit[1]
Maximum number of instructions/clock	4 or 8	100s to 1000s
Ease of programming	C,C++ software flow	HDL hardware flow
I/O flexibility	Limited	Flexible
Memory management	Built-In	Manual
Memory bandwidth	1-Gbps SDRAM	9.5-Gbps DDRII[2]
Power consumption (for high-end processing devices)	Low per device (high per computation)	High per device (low per computation)

(1) Multipliers Can Be Implemented Using Hardware (HW) Based Multipliers & Logic Element (LE) Based Multipliers.
(2) Other Memory Interfaces are Supported Including Single Data Rate, Double Data Rate, RLDRAMII, QDR & QDRII

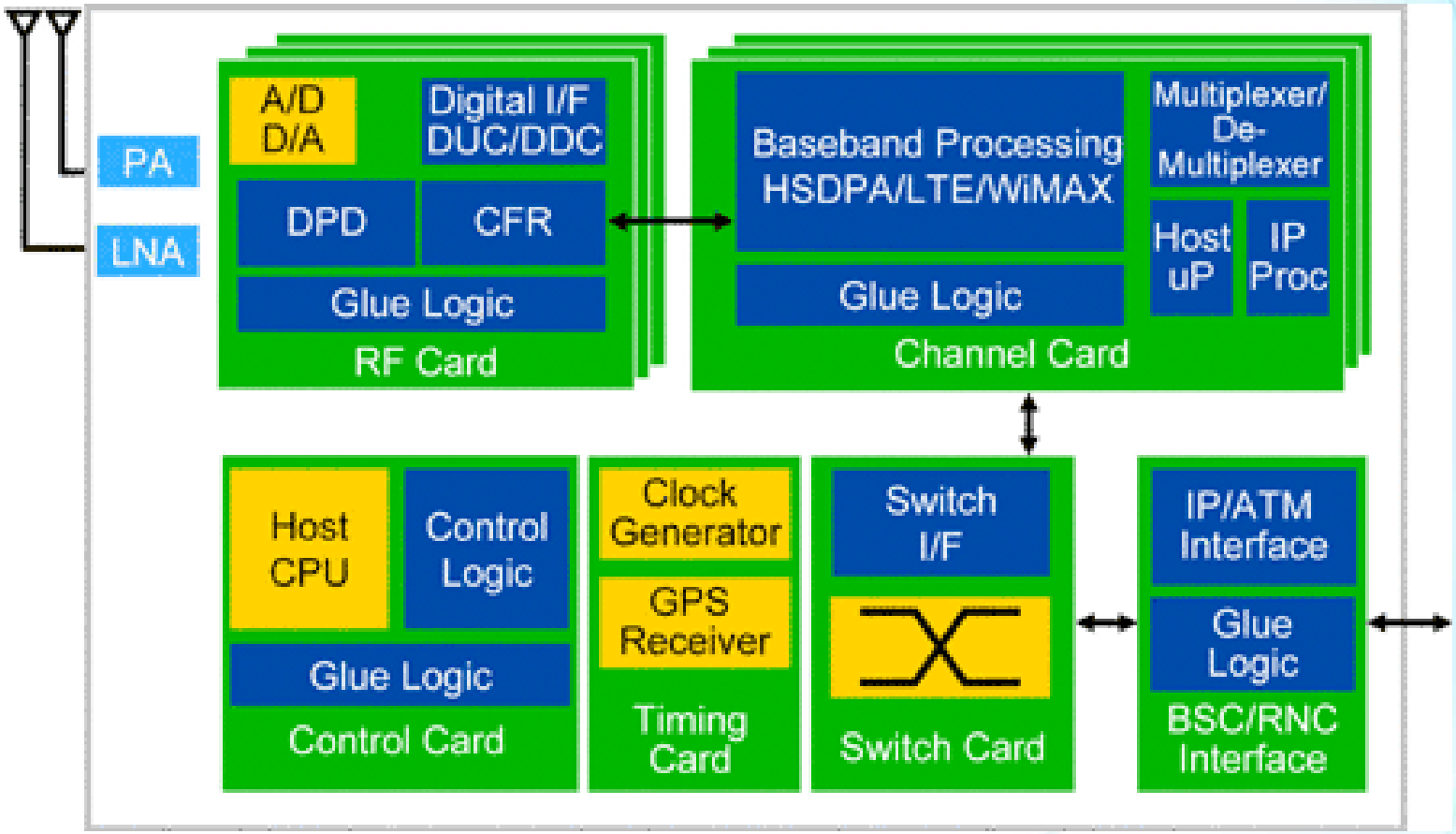
Datapath Processing Architecture Options



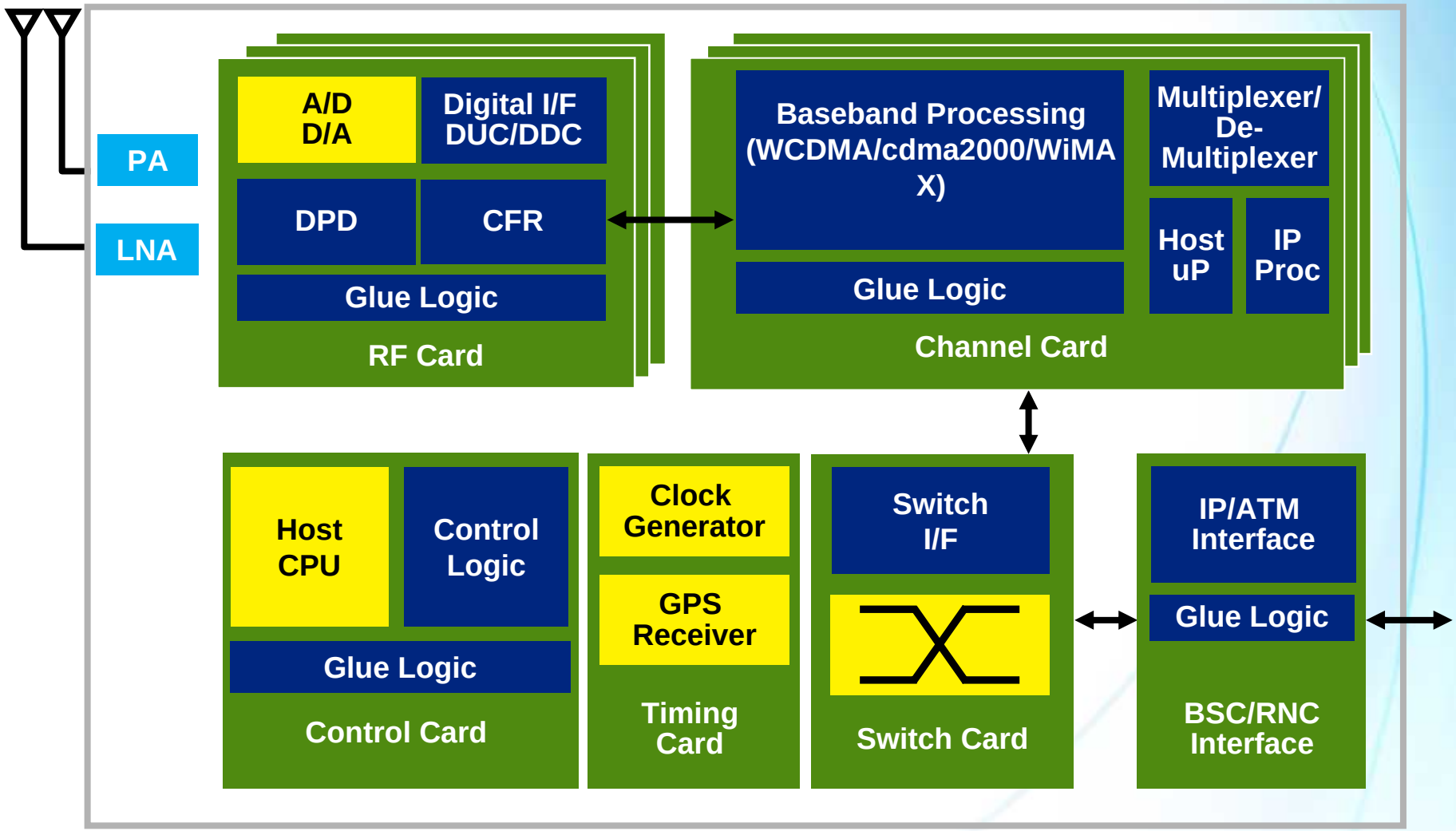
Example: Wireless Tester



Example: WiMAX Channel Card

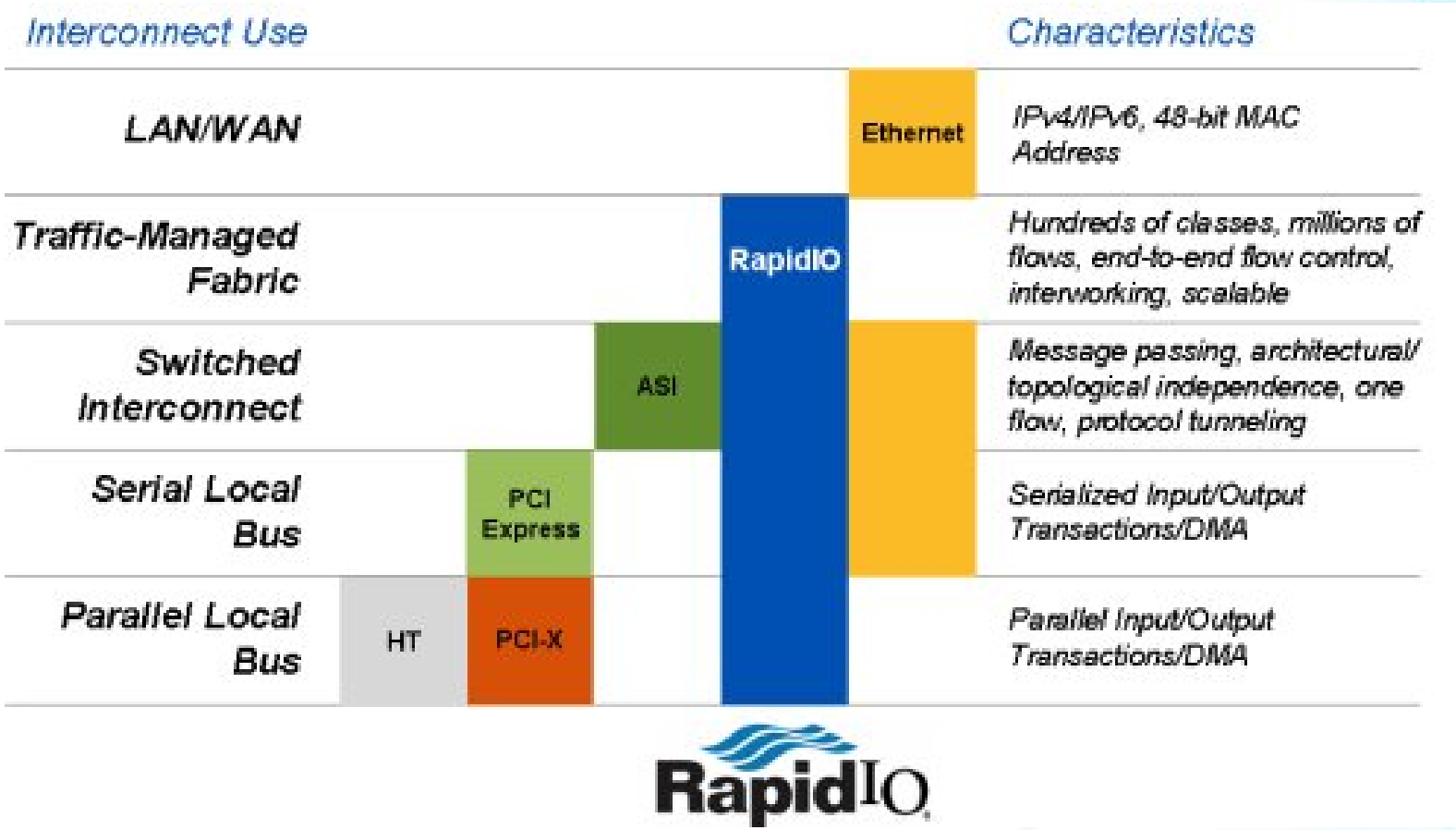


Example: WiMAX Channel Card

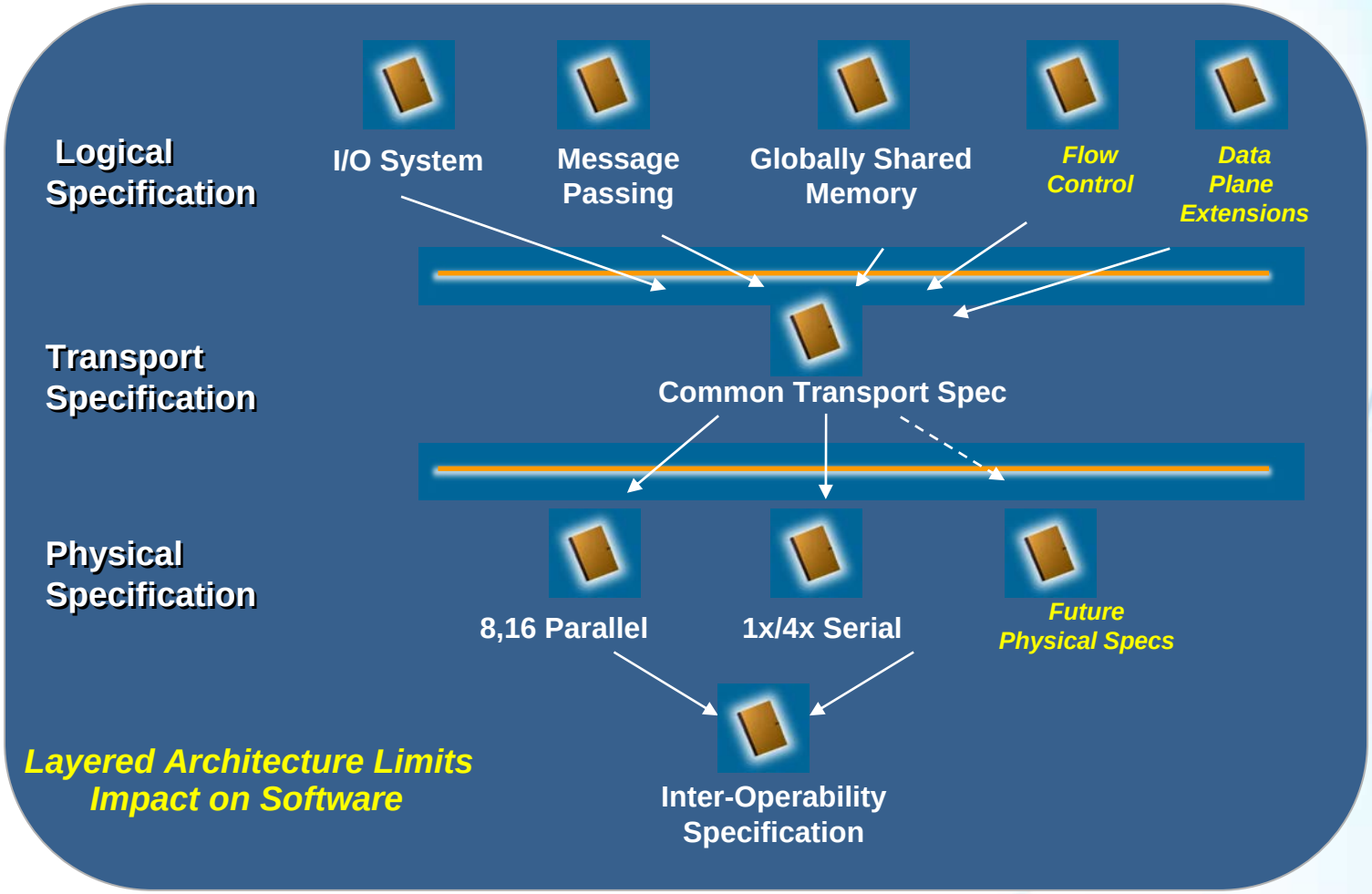


Serial RapidIO Review

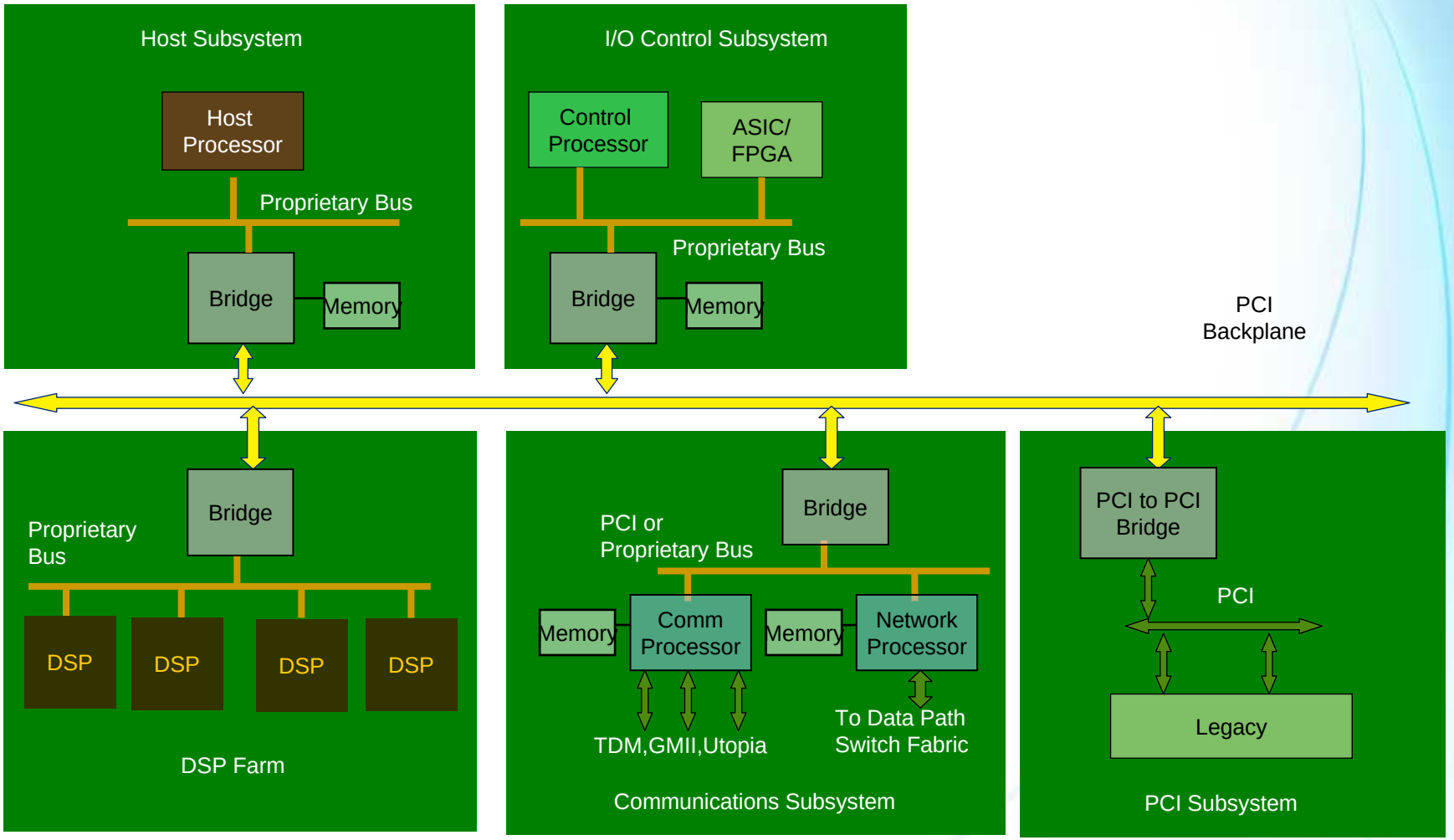
Interconnect Technology Review



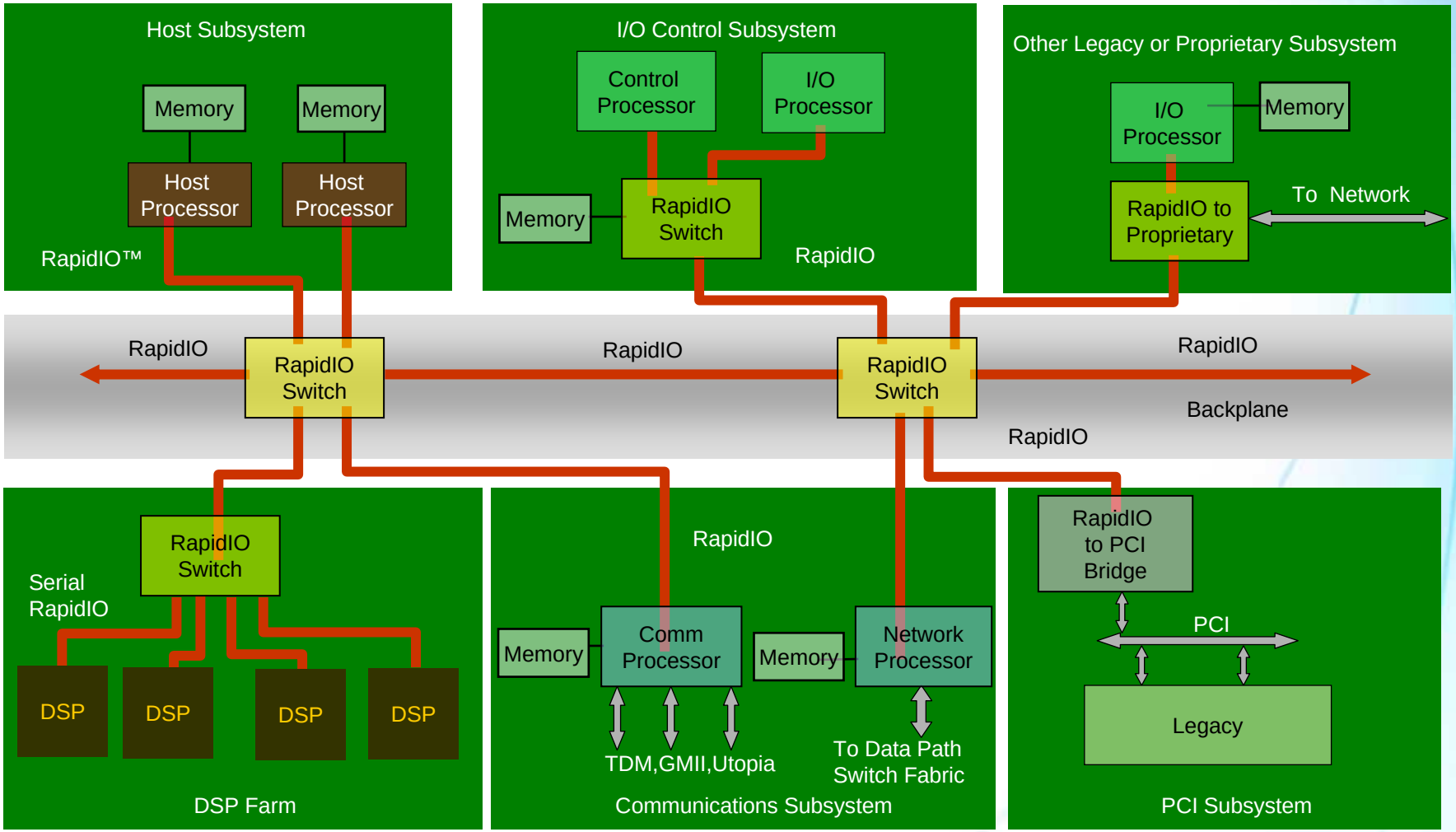
RapidIO Hierarchy



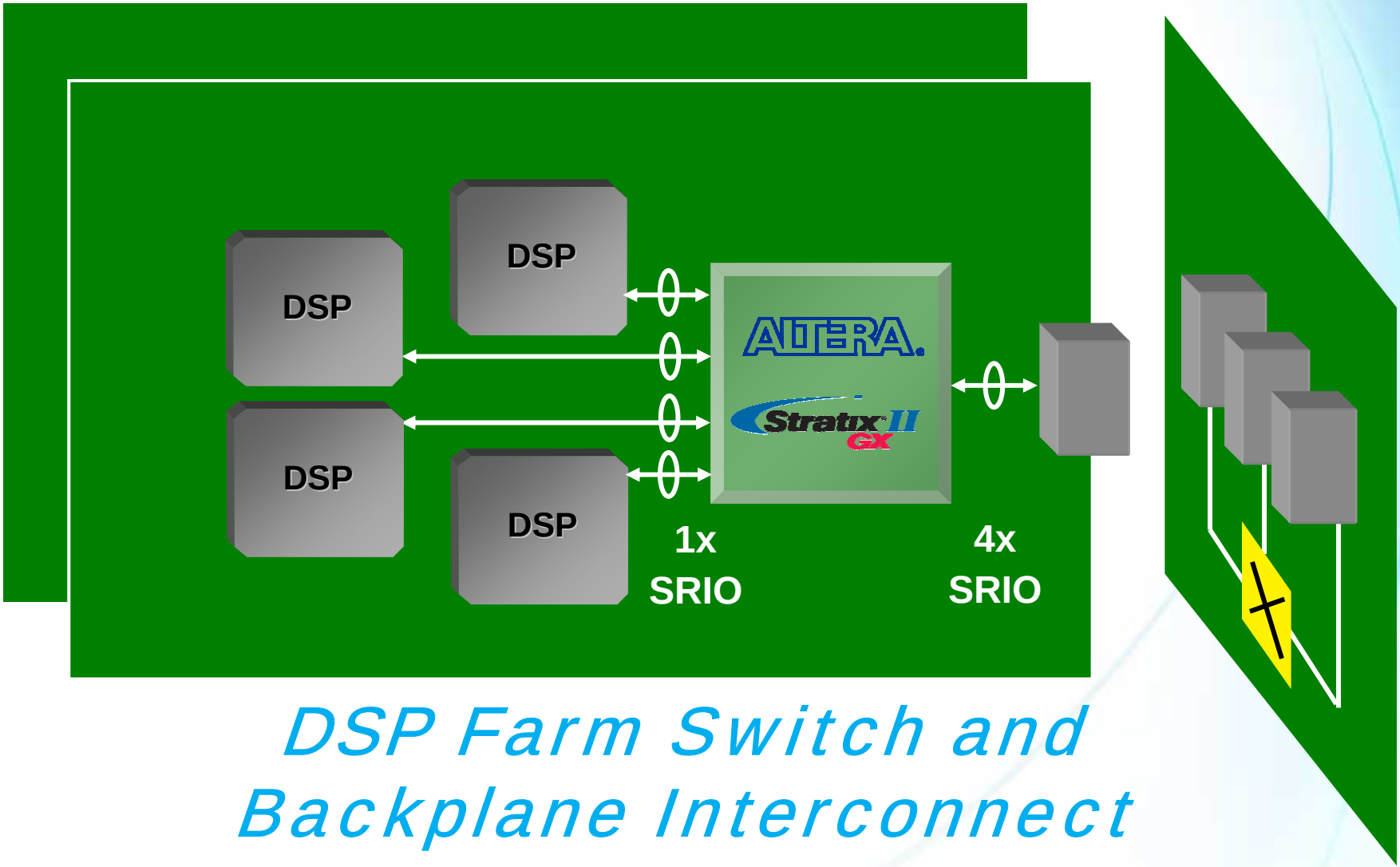
Traditional Interconnect Architecture



RapidIO Systems

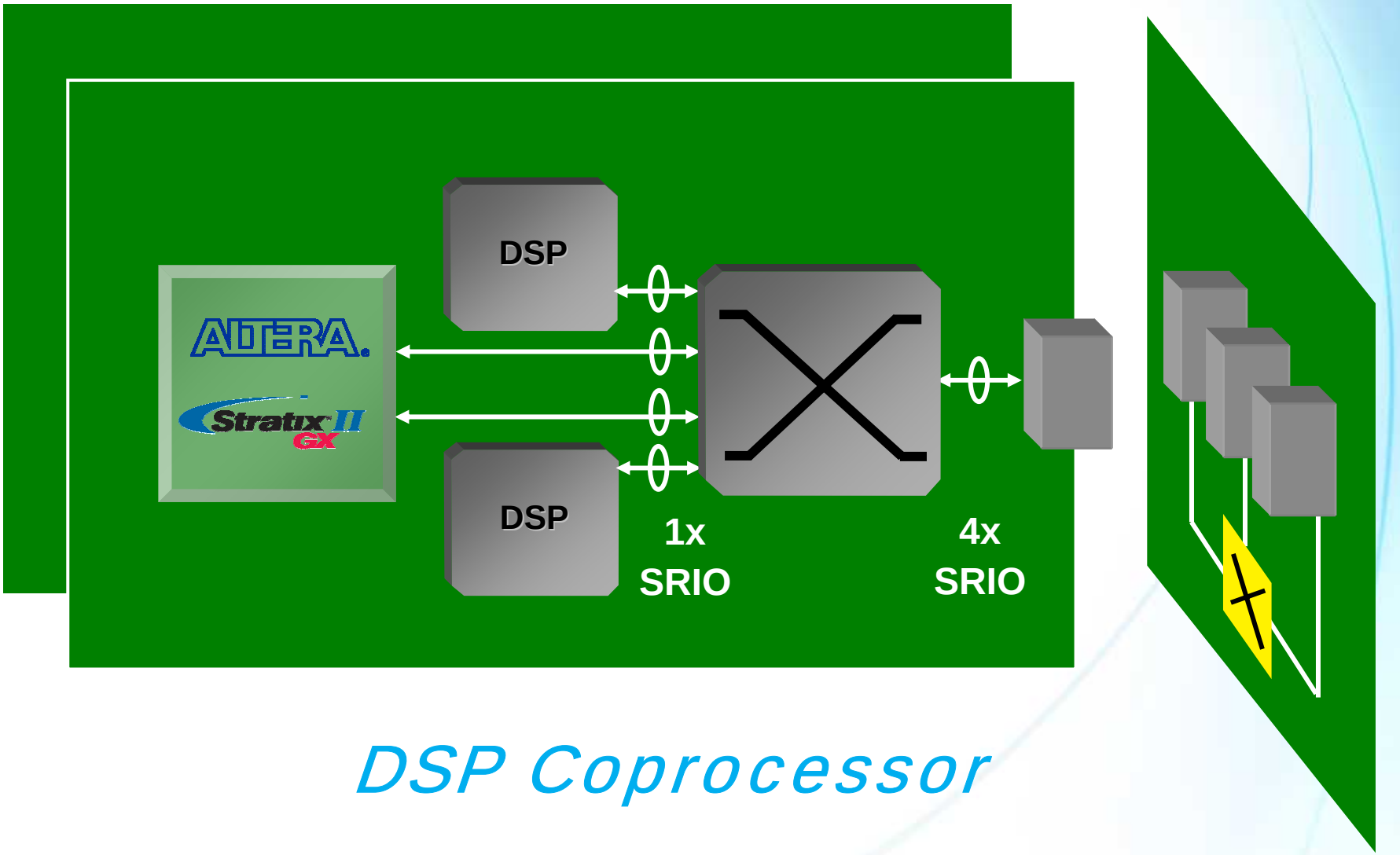


Typical Application



DSP Farm Switch and Backplane Interconnect

Typical Application



DSP Coprocessor

Altera Serial RapidIO Solution

Altera Stratix II GX RapidIO Solution

- RapidIO MegaCore® Version 6.1
- Compliant with RapidIO Trade Association, *RapidIO Interconnect Specification*, Revision 1.3
- Physical layer features
  - 1x/4x serial
    - Stratix® II GX support, including 1x and 4x up to 3.125 Gbps
    - Cyclone® II, Stratix II, Stratix III, and HardCopy® II support with an XGMII-like interface to a high-speed full-duplex, serializer / deserializer (SERDES) transceiver
  - 8-bit parallel
- Transport layer features
  - Supports multiple logical layer modules
  - Supports 8-bit device identities (IDs)
  - Device IDs, addressable CARs, and CSRs eliminate hop-count handling and CRC recomputing
- Logic layer features
  - Maintenance master and slave logical layer module
  - I/O master and slave logical layer module
  - Doorbell support
- PCI Express development kit expansion via HSMC connectors to AMC module
- SRIO loopback example design available based on the signal integrity kit
- Other IP vendors: Mercury Computers, GDA Technologies, Jennic, Preasum

SRIO Stratix II GX Characterization

- SRIO I/O (*PMA*) specifications have evolved
  - Currently identical to XAUI @ 3.125 Gbps
  - Currently identical to Gigabit Ethernet @ 1.25 Gbps and 2.5 Gbps
- Stratix II GX passes SRIO characterization spectacularly at 3.125 Gbps
- The XAUI and SRIO characterization report now available

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Interoperability

- Stratix II GX with Altera MegaCore interoperability with TI DSP device via SRIO
  - Stratix II GX signal integrity (SI) board to TI DSP 6455 board via an SMA breakout board

Number of Lanes	Baud Rate (Gbaud)	Internal Data Path Width
X1	1.25	32
X1	2.5	32
X1	3.125	32
X4	2.5	64
X4	3.125	64

- Interoperability with IDT switch x1 @ 3.125 Gbps
- Bittware AMC board with Stratix II GX interoperability with TI DSPs via Tundra passed

Stratix II GX FPGA-based Serial RapidIO Solution

Item	Status
Stratix II GX FPGA	☑
IP core (x1, x4 serial, x8 parallel)	☑
Development kit	☑
Reference designs	☑
Device characterization report	☑
System validation report	☑
Additional interoperability (Texas Instruments)	☑

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Summary

- Serial RapidIO has become the interface of choice for high-performance DSP applications
- Altera offers complete, easy-to-use Serial RapidIO solutions
  - Arria™ GX FPGAs for mainstream applications
  - Stratix II GX FPGAs for high-performance systems
- Low-risk, hardware-verified solutions
  - Stratix II GX interoperability with Texas Instruments
  - Development boards

Fastest Time-To-Market with Reliable RapidIO Solutions

Serial RapidIO Demo