7 Single Pulser

Despite its small size, this circuit has shown to be hard to specify in many formalisms like temporal logics and is well-suited as an introductory example.

7.1 Introduction

A Single Pulser is a clocked-sequential device with a one-bit input, *I*, and a one-bit output *O*. The purpose of the circuit is described as follows [WiPr80]:

> We have a debounced push-button, on (true) in the down position, off (false) in the up position. Devise a circuit to sense the depression the button and assert an output signal for one clock pulse. The system should not allow additional assertions of the output until after the operator has released the button.

A design specification of the Single Pulser can be found in the text book “The Art of Digital Design” by D. Winkel and F. Prosser [WiPr80]. A detailed treatment of this example for comparing different specification formalisms can be found in [JoMC94].

7.2 Specification

Assuming that the input is synchronous and debounced, the specification may be stated as:

> For each input pulse on *I*, the Single Pulser issues exactly one pulse of unit duration on *O* regardless of the duration of *I*.

The specification may be also stated by the following three properties [JoMC94]:

1. Whenever there is a rising edge at *I*, *O* becomes true some time later.
2. Whenever *O* is true it becomes false in the next time instance and it remains false at least until the next rising edge on *I*.
3. Whenever there is a rising edge, and assuming that the output pulse doesn’t happen immediately, there are no more rising edges until that pulse happens (There can’t be two rising edges on *I* without a pulse on *O* between them).

In [JoMC94] the specification is given in different formalisms like PVS and CTL [ORSS94, ClEm81].

7.3 Implementation

The implementation is taken from [WiPr80]. The incoming, not yet debounced asynchronous signal **`Pulse_In`** is fed to a D flip_flop and thus becomes the synchronized signal **`Pulse_sync`**, which is then delayed for one clock cycle by using another D flip-flop. Its output is negated, and the AND-connection of the synchronous pulse with its own delay generates the resulting, one clock-cycle lasting signal **`Pulse_Out`** (Fig. 7-1).

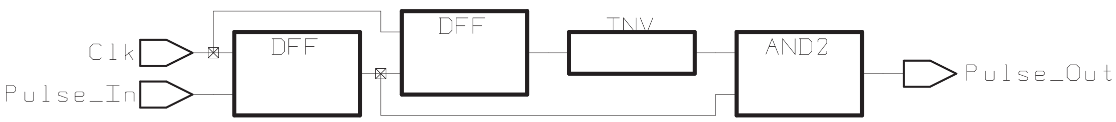

Figure 7-1: Single Pulser

In Fig. 7-2 waveforms are given to illustrate the behavior of the circuit.

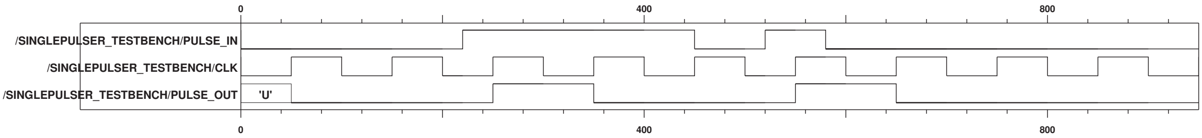

Figure 7-2: Example waveform

7.4 Status and Acknowledgments

The circuit has been originally proposed by J. Staunstrup. Most of the actual text is directly quoted from [Stau93]. Thanks to C.-J. Thomas for creating the VHDL description.

7.5 Literature

[ClEm81] E.M. Clarke and E.A. Emerson. Design and Synthesis of Synchronization Skeletons using Branching Time Temporal Logic. In D. Kozen, editor, *Proceedings of the Workshop on Logics of Programs*, volume 131 of *Lecture Notes in Computer Science*, pages 52–71, Yorktown Heights, New York, May 1981. Springer-Verlag.

[JoMC94] S.D. Johnson, P.S. Miner, and A. Camilleri. Studies of the single pulser in various reasoning systems. In T. Kropf and R. Kumar, editors, *Proc. 2nd International Conference on Theorem Provers in Circuit Design (TPCD94)*, volume 901 of *Lecture Notes in Computer Science*, pages 126–145, Bad Herrenalb, Germany, September 1994. Springer-Verlag. published 1995.

[ORSS94] S. Owre, J.M. Rushby, N. Shankar, and M.K. Srivas. A tutorial on using PVS for hardware verification. In T. Kropf and R. Kumar, editors, *Proc. 2nd International Conference on Theorem Provers in Circuit Design (TPCD94)*, volume 901 of *Lecture Notes in Computer Science*, pages 258–279, Bad Herrenalb, Germany, September 1994. Springer-Verlag. published 1995.

[Stau93] J. Staunstrup. IFIP WG 10.2 Collection of Circuit Verification Examples, November 1993.

[WiPr80] D. Winkel and F. Prosser. *The Art of Digital Design*. Prentice-Hall Inc., 1980.