10   Counters

Counters are basic building blocks in digital systems. A counter can be constructed in multiple ways. In this lab we will use the register of the previous lab to construct a 4-bit binary up counter.

Note: This lab has Altera Maxplus simulation requirements. Please see the prelab sheet.

I. Devices needed

You will need two 7474 ICs, a PLD that implements a 2/1 4-bit mux, a PLD that implements a 4-bit binary adder, and perhaps some 74XX gates for glue logic. The pinout for the 4-bit binary adder is:

- Pin 12 – GND, Pin 24 - Vcc.
- Four bit A input: A(3): pin2, A(2): pin3, A(1): pin4, A(0): pin5
- Four bit B input   B(3): pin6, B(2): pin7, B(1): pin8, B(0): pin9
- Carry-In : pin 10
- Four Bit Sum output: Sum(3): pin22, Sum(2): pin21, Sum(1): pin20, Sum(0): pin19
- Carry Out: pin 18

Unused inputs on the PLD can be left unconnected. The pinout for the 2/1 4-bit mux function can be found in the previous lab. Your TA will program your PLDs.

II. 4-Bit Register with Up counting capability

Use the devices listed above to implement the 4-bit register with up counting capability as shown below.
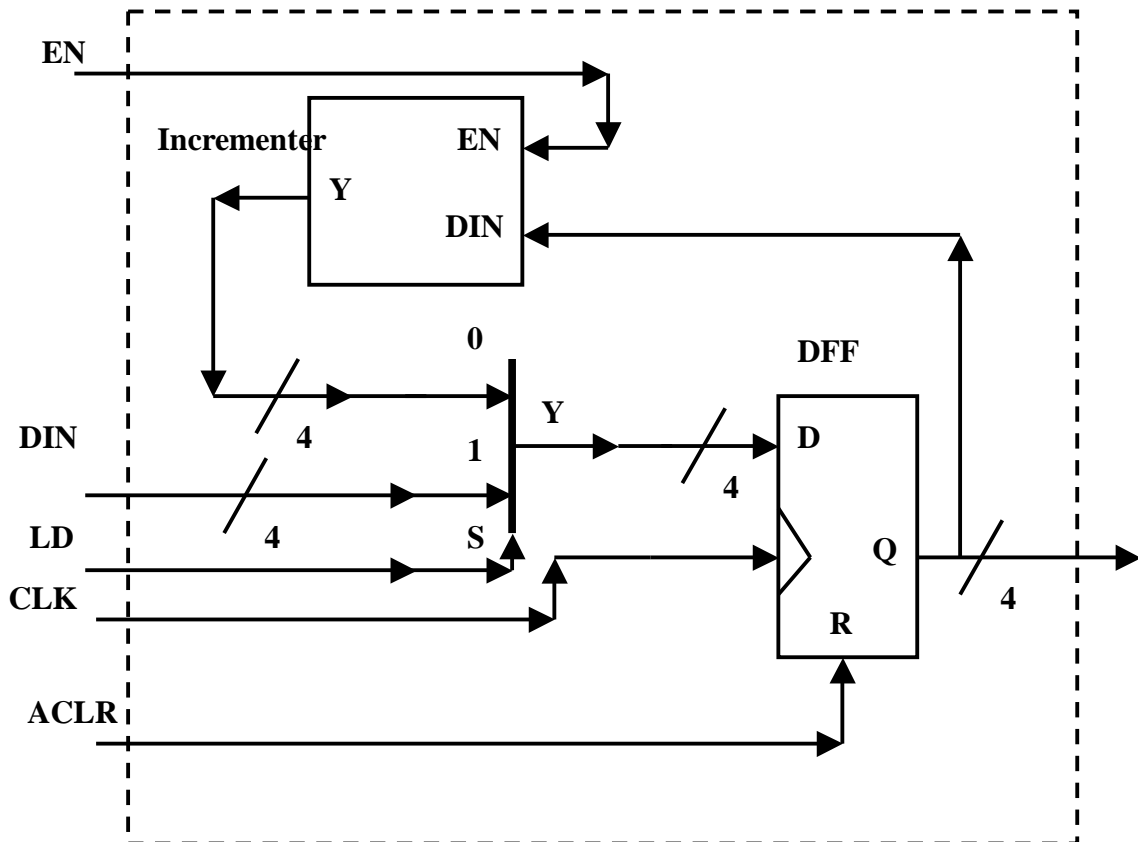
The details of the schematic are for you to determine!!!. You may use all or some of the integrated circuits listed in Section I. You will need to determine how to implement the incrementer capability using the 4-bit binary adder supplied by the TA (when EN=0, Y = DIN, when EN=1, Y = DIN+1)

A. Connect the DIN 4-bit bus to data switches and verify that register can be loaded, and can be asynchronously cleared.

B. Asynchronously clear the register, then verify that the counter will count from 0 to 15, and then wrap around to 0, with the counter advancing on each clock that LD is held active.

C. The longest delay in the counter will occur when CNT= "1111" and the counter increments to "0000". The delay path components for maximum frequency of operation are the CLK2Q through the DFFs, the incrementer delay, the 2/1 Mux

delay, plus the setup time of the DFFs. All of the delay values except the PLD adder delay can be determined from data sheets (the delay of the 2/1 Mux PLD was determined in the previous lab - it will be *Tpd* from the PLD data sheet). Construct a separate circuit for your incrementer in which the worst case delay can be measured (measure the delay from enable going from LOW to HIGH with DIN="1111"to the MSB of Y going low). Use the oscilloscope with your circuit to measure this worst case delay through the incrementer.

III. Report

A. Give a complete schematic of your design.
B. Show the circuit used for determining the worst case incrementer delay and give the measured value.
C. Using the delay components mentioned in C, part II, give the maximum frequency of operation of this counter in MHz (1/(longest delay path). Be sure to show where you got the delay values from the datasheets for the 74XX components.

PRE LAB DATA SHEET   **TA CHECKOFF _____**

A. The ZIP archive with this lab contains a MAXPLUS schematic called CNT4 that implements the circuit shown in PartII. Two simulation waveform files are provided: *cnt4_gold.scf* and *cnt4.scf*.   Your task is to edit the *en*, *ld*, and *aclr* inputs on the *cnt4.scf* waveform such that the *dout[3..0]* waveform duplicates the *dout[3..0]* waveform found in the *cnt4_gold.scf*. This will require you to compile the *cnt4.gdf* schematic and simulate it after you have edited the *cnt4.scf* waveform. You may NOT CHANGE the *din[3..0]* waveform.   The default device for the *cnt4.gdf* file has been set to the *Classic* family, AUTO choice -- do not change this.

To make your job easier, it is possible to compare two waveform files. To compare two waveforms, use the "View→Fit In Window" command to view the entire waveform (do this on both *cnt4.scf* and *cnt4_scf*). Click on the *cnt4.scf* window to select it, then use the File→Compare menu option to compare the *cnt4.scf* waveform to the *cnt4_gold.scf* waveform. Any differences in the *dout[3..0]* waveform will show up in black. You must have a printout of your new waveform at the beginning of lab for TA signoff (or demo to the TA via a portable PC).

B. Draw a detailed schematic for your 4-bit register using the devices given.

C. Show the circuit that you will use for measuring worse case incrementer delay and discuss how you will the oscilloscope to make this measurement.

LAB DATA SHEET

A. Working 4-bit register (both synchronous load and asychronous clear)

        TA CHECKOFF _____

B. Working up counting capability of the register.

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C. Measured worst case incrementer delay _____ (in ns)

D. Sketch of waveforms used to measure worse case incrementer delay.

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