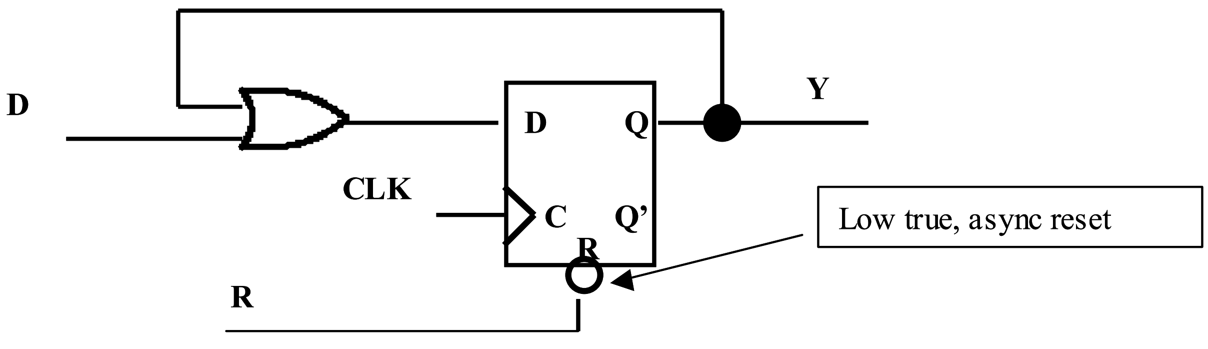
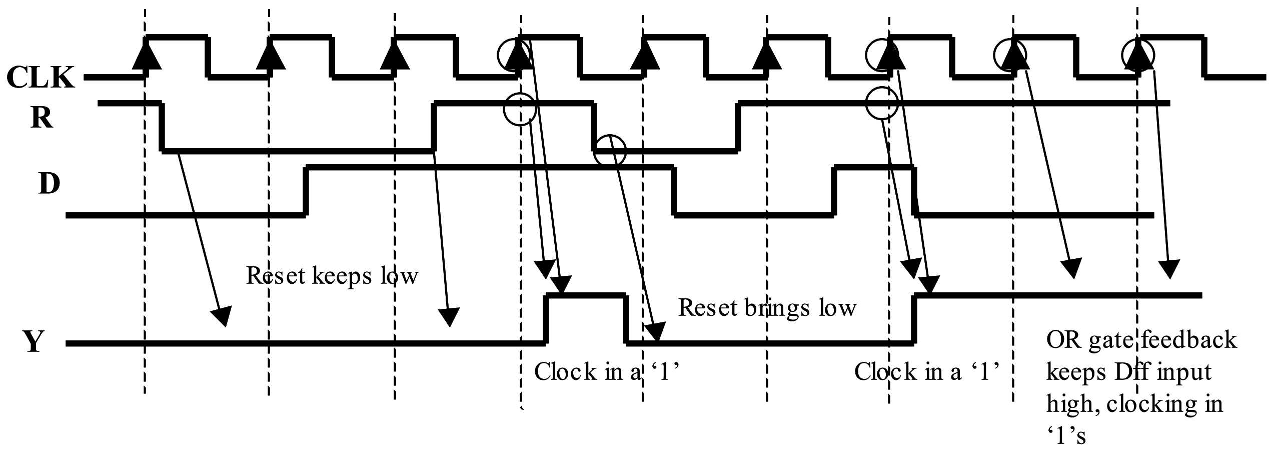
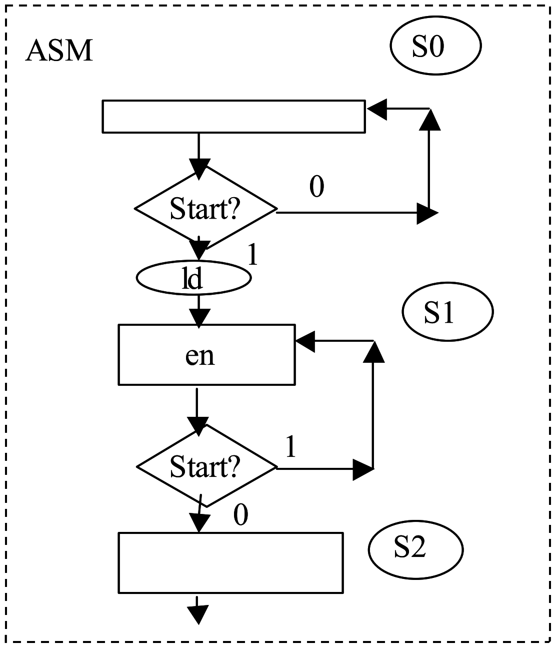
EE 4743 Test #1 – Fall 2002 Solutions

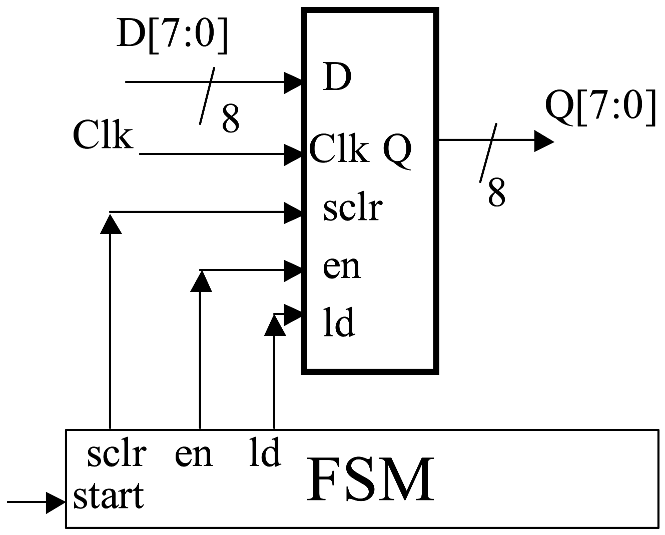
1. (15 pts) On the diagram below, complete the timing diagram for the Y output for all clock cycles.

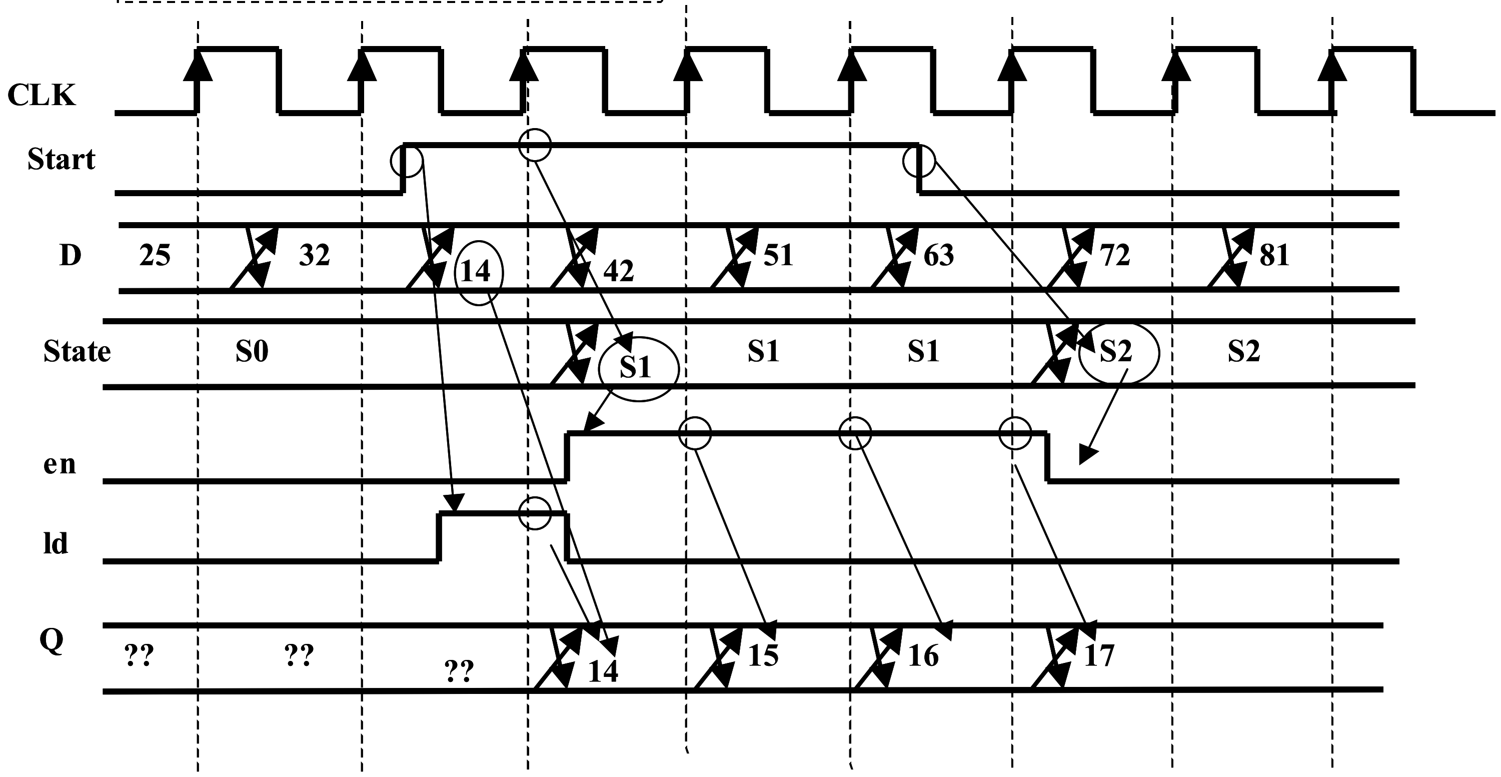




2. (15 pts) On the waveforms below, complete the waveforms for State, ld, en, and Q. The FSM is controlling an UP counter .



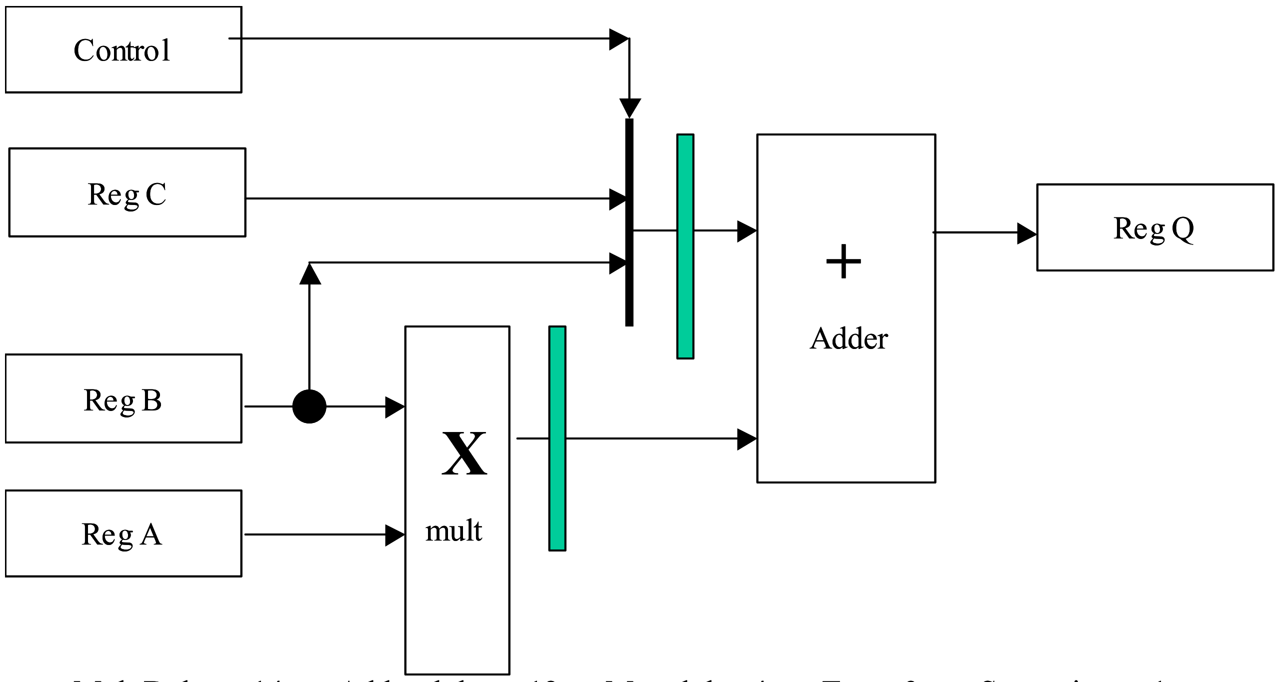




3. (15 pts) For the figure below:

   a. Give the maximum register-to-register delay. Show your work.
   Tcq + tmult+ tadder + tsu = 3 + 14 + 12 + 1 = 30 ns

   b. Modify the diagram to add one level of pipelining but still maintain the same functionality. Add the pipeline stage in the place that will **improve the register-to-register delay the most**. *Compute the new maximum register-to-register.* Assume that adding a pipeline registers to any functional unit (adder, multiplier, or mux) breaks the combinational delay path in the unit exactly in half.



Mult Delay = 14ns, Adder delay = 12ns, Mux delay 4 ns, Tcq = 3 ns, Setup time = 1 ns, Hold time = 2 ns

Longest path: tcq + Tmult + Tsu = 3 + 14 + 1 = 18 ns.

Path through adder: tcq + tmult + Tsu = 3 + 12 + 1 = 16 ns.

IF the pipeline stage is placed in the middle of the multiplier, then a slower system results!

Longest path = tcq + ½ Tmult + Tadder + Tsu = 3 + 7 + 12 + 1 = 23 ns!! Not the best solution.

4. (15 pts) The figure below is the Flex 10K logic cell. The delays in boxes are the delays for each associated element. Show work for extra credit.

a. Compute the setup time for DATA1 relative to clock Pin LABCTRL3 . Assume the delays shown (note that carry chain block and cascade chain contribute to delays even if they are not being used). The setup time is for the path to the D-input of the DFF.
Tsu + Tmax Data1 to D path - Tmin (Clock path) = 1 + 6 + 1 + 1 + 2 – 3 = 8 ns

b. Compute the hold time for DATA1 relative to clock Pin LABCTRL3. The hold time is for the path to the D-input of the DFF.
Thd + Tmax Clock Path - Tmin (Data1 to D path) = 2 + 3 –(6+ 1 + 1 + 2) = -5 ns

c. Compute the clock-to-out time for output F from a clock edge arriving at LABCTRL3.
Tclock select+ Tcq + Out mux delay = 3 + 3 + 2 = 8 ns

d. Compute the combinational pin-to-pin delay for DATA1 to output F
Tlut + Tcarry chain + T cascad + Tmux = 6 + 1 + 1 + 2 = 10 ns

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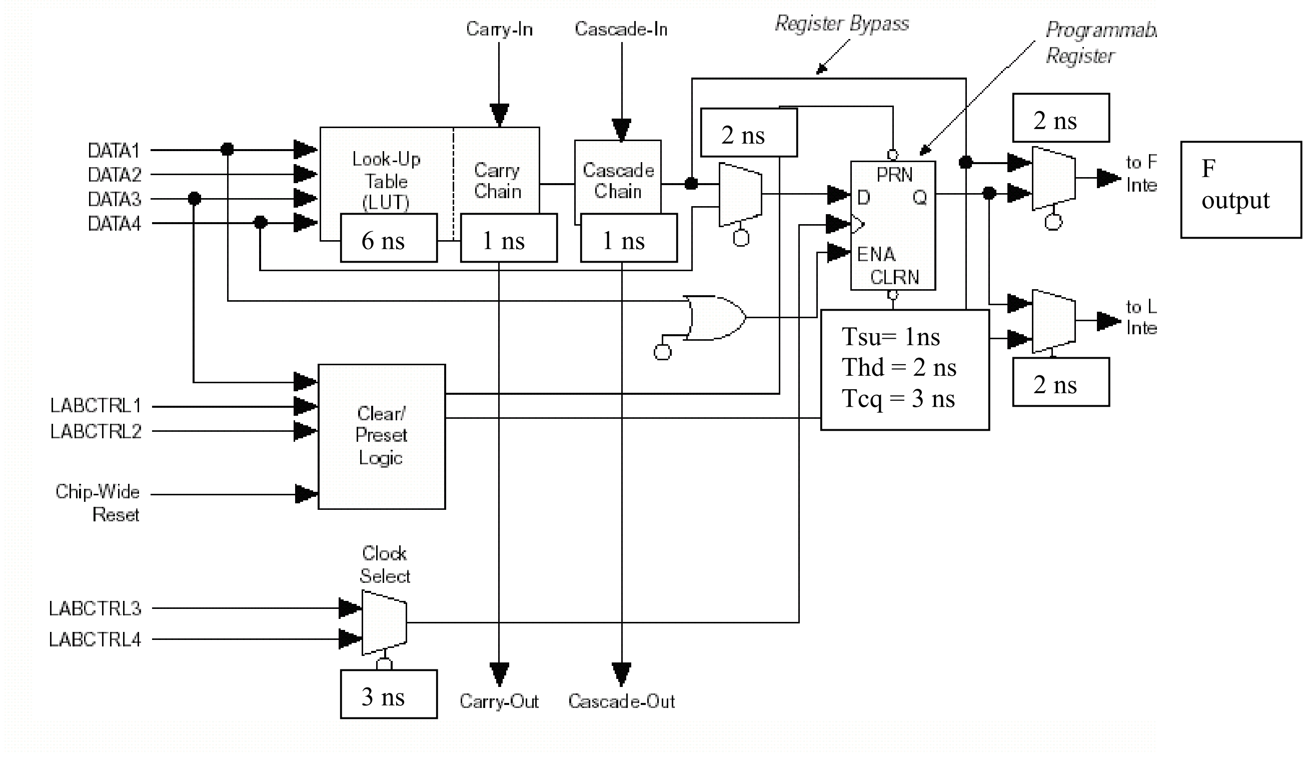
Figure 6. FLEX 10K Logic Element



5. (5 pts) Joe Schmoe from Ole Miss attempted to write the VHDL for a 2-1 mux and the sorry mess is shown below. Please correct it (maintain the 'process' block format, do not just write the Boolean equation for a 2-1 mux).

~~Y <= A;~~

```
Process  (A, B, S)

  begin

    Y <= A;
    if ( S  =  '1')   then

         Y  <= B;
    end if;
 end process;
```

6. (5 pts) A Flex 10K input/output cell has a DFF included in it. Why is there a DFF in the Input/output cell? Why not just use a DFF in the logic cell?

   Placing DFFs in the Input/Output cell minimizes setup time for external inputs, and Clock-to-out for external outputs.

7. (4 pts) Give two reasons why dedicated RAM blocks are included on FLEX10K FPGAs. Why not just build the RAMS using the lookup tables that are in each logic cell?

   RAMs built from LUTs are slower and take more area than dedicated RAMs.

8. (4 pts) Explain what is done in the FLEX10K logic cell to improve the implementation of adders.

   Dedicated logic for carry generation (the carry chain) was placed in each logic cell.

9. (4 pts) Give the decimal value for the 8-bit number 11010000 encoded as 2.6 Fixed point number

   11 . 010000 = 3 + 0.25 = 3.25

10. .(4 pts) What is the 8 bit sum of 81h + FEh in signed saturation addition mode?

   81h + Feh = 7Fh using normal addition, which is an overflow. Because both operands are negative, then saturate to maximum negative value which is 80H.

11. (4 pts) What is the 8 bit sum of 81h + FEh in unsigned saturation addition mode?

    81H + FEH = 7Fh which produces a carry out of the MSB which is unsigned overflow. Saturate to maximum unsigned value which is FFh.

12. (10 pts) We discussed the differences between ASICs and FPGAs for implementation technologies.
    a. Give 2 reasons why an implementation in an ASIC be desirable over an FPGA?

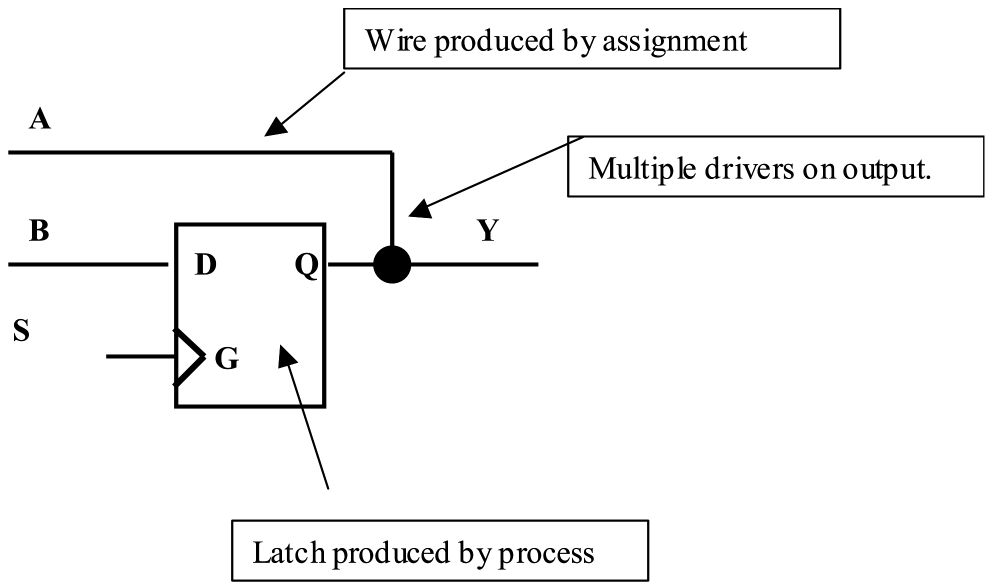
       ASICs are faster than FPGAs, much cheaper on a per-unit-cost after NRE costs are recovered (if you need a lot of chips), and offer much higher density.

    b. Give a reason why an FPGA implementation might be desirable over an ASIC implementation. (this reason cannot be the Boolean negation of the reasons given in (a)).

       FPGAs give you the ability to fix problems in the field by simply reprogramming them, also have zero turnaround on designs in need something fast.

BONUS (4 pts)

For problem #5, draw the logic that is synthesized for Joe Schmoe's original code.


Wire produced by assignment
A
Multiple drivers on output.
B
Y
D
Q
S
G
Latch produced by process