Table A-20 strengths

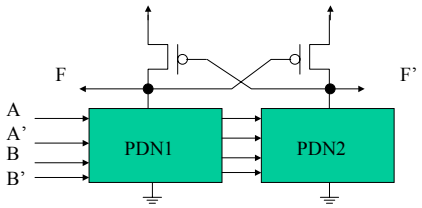
value	%v	drive0	drive1	Description
0	Hi	highz0	highz1	High impedance
1	Sm	-	-	Small capacitor
2	Me	-	-	Medium capacitor
3	We	weak0	weak1	Weak drive
4	La	-	-	Large capacitor
5	Pu	pull0	pull1	Pull drive
6	St	strong0	strong1	Strong drive
7	Su	supply1	supply0	Supply drive

Table A-21 Switch Strength Reduction

Input Strength	Ideal Device Output Strength	Resistive Device Output Strength
supply	strong	pull
strong	strong	pull
pull	pull	weak
weak	weak	medium
large	large	medium
medium	medium	small
small	small	small
high impedance	high impedance	high impedance

Differential Logic

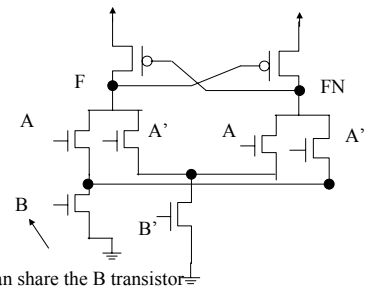
DCVSL – Differential Cascade Voltage Switch Logic



Both PDN networks are never conducting at same time

We can reduce transistor count by sharing transistors.

Xor gate with shared transistors



Can share the B transistor

HW Assignment

- Zip archive has verilog file *tb_xorgate_dcvsl.v, xorgate_dcvsl.v*
  - Tb_xorgate_dcvsl.v is testbench for XOR gate
  - xorgate_dcvsl.v has empty module named xorgate_dcvsl
- Complete switch level model of xorgate_dcvsl
  - Be careful of drive strengths.
  - A *supply* strength going through a pmos/nmos always comes out as strong strength.
  - A supply strength going through a rpmos/rnmos comes out as pull strength

Supply strength

pmos

strong strength

Supply strength

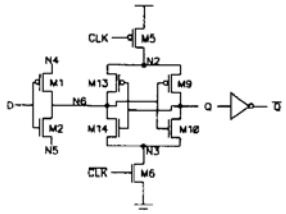
rpmos

pull strength

Dual Edge Triggered Flip-Flop Model

- Write a Verilog transistor level model that simulates the DETFF on the next two pages
  - The DETFF consists of two modules which must be connected together
  - Zip archive has *detff.v* (fill this module in) and *tb_detff.v* (testbench).
  - There is also a link for a sample Makefile.
- In my model, I had to use delays at a couple of nodes in order to get the model to function correctly (there are solutions that do not require delays).
  - I also had to use strength reduction transistors in a couple of places
  - There are multiple correct solutions to this problem
  - You must understand how the DETFF works before trying to model it.

Module A of Dual Edge Triggered Flip-Flop [1]



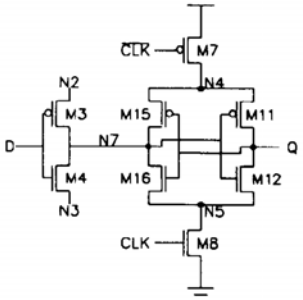
(a)

SIZE (w/l in microns)	
M1	4/1.6
M2	4/1.6
M5	8/1.6
M6	8/1.6
M9	4/2.6
M10	4/2.6
M13	8/1.6
M14	8/1.6

Transistor sizes give strength hints

[1] A. Gago, "Reduced Implementation of D-Type DET Flip-Flops, IEEE Journal of Solid-State Circuits, Vol 28, No 3., March 1993

Module B of Dual Edge Triggered Flip-Flop



(b)

SIZE (w/l in microns)	
M3	4/1.6
M4	4/1.6
M7	8/1.6
M8	8/1.6
M11	4/2.6
M12	4/2.6
M15	8/1.6
M16	8/1.6

Simulation of DETFF