Transistor Sizing for Minimizing Power Consumption of CMOS Circuits under Delay Constraint

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Abstract

We consider the problem of transistor sizing in a static CMOS layout to minimize the power consumption of the circuit subject to a given delay constraint. Based on our characterization of the short circuit power dissipation of a CMOS circuit we show that the transistors of a gate with high fan-out load should be enlarged to minimize the power consumption of the circuit. We derive analytical formulation for computing the *power optimal* size of a transistor and isolate the factor affecting the power optimal size. We extend our model to analyze power-delay characteristic of a CMOS circuit and derive the *power-delay optimal* size of a transistor. Based on our model we develop heuristics to perform transistor sizing in CMOS layouts for minimizing power consumption while meeting given delay constraints. Experimental results (SPICE simulations) are presented to confirm the correctness of our analytical model.

1 Introduction

Transistor sizing is a very effective way to improve the delay of a circuit. Earlier approaches for transistor sizing formulated the problem as that of minimizing the area of the circuit subject to certain delay constraint or optimizing the area-delay product [10, 4, 5, 16, 11, 7, 8, 15]. With improved process techniques and reduced feature sizes the constraint on area is becoming less strict; on the other hand, the growing market of low-power electronics is pushing the constraint of power consumption to the top of the stack of priorities. Most of the existing methods assume that the power consumption of a circuit is proportional to the "active area" of the circuit. Therefore they assume that minimizing the active area also minimizes the power consumption of the circuit.

Recent studies have revealed that the power consumption of a static CMOS circuit is not necessarily minimized by minimizing the active area, but, can be improved by enlarging some of the transistors driving large loads[1, 9]. Hence, a proper understanding of the issues of power consumption with respect to transistor sizing is essential to be able to optimize the power consumption of a circuit while meeting a given delay budget. In this paper we develop an analytical model for the power consumption of a CMOS circuit based on the analysis of short circuit power consumption given in [17] and the delay model of [6] and isolate the factors that affect the power consumption of a circuit.

We derive the 'power optimal' and the 'power-delay optimal' size of a transistor analytically with actual circuit simulation results to confirm the validity of our formulation. We analyze the main factors that affect the power optimal and power-delay optimal size of a transistor in a gate. We present analytical methods to minimize the power consumption of a layout by sizing the transistors to their power optimal size. We also develop techniques to generate high-performance layouts with minimal increase in power consumption. Note that by judicious transistor sizing with the power-delay optimization as the objective, we are avoiding unnecessarily large transistors and hence also minimizing the 'active area' for the circuit.

The rest of the paper is organized as follows. Section two presents the formulation and analysis of the power optimal and power-delay optimal transistor sizing problem along with SPICE simulation results to verify the correctness of the model. We describe our heuristics for optimizing power consumption subject to delay constraint in section three. We show results from a few real circuit layouts to demonstrate the usefulness of our heuristics in section four. Section five concludes with comments on further research.

2 Analysis of power and power-delay product

We use CMOS inverters in our analysis for simplicity. We extend our analysis to general CMOS gates in section 2.2.

2.1 Analytical formulation for power consumption

The power consumption of a single static CMOS gate, neglecting the static power consumption, is composed of P_{cap}, the capacitive power due to charging and discharging of capacitors and P_{sc}, the short circuit power dissipated when both the p-type and the n-type blocks are conducting simultaneously during a transition. The capacitive power is well understood, and is given by

$$P_{cap} = C_L V^2 f \quad (1)$$

where C_L is the total load capacitance of the gate. V is the supply voltage and f is the frequency of transition.

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The short circuit power dissipation, P_{sc} is given by the following expression [17]:

$$P_{sc} = \frac{\beta}{12}(V - 2V_T)^3 \frac{\tau}{T}. \quad (2)$$

Here, β is the gain-factor of the transistor, V_T is the threshold voltage and τ is the input transition time. $T = 1/f$, is the time period.

We assume in the following analysis that the channel length of the transistors is fixed and the size of the transistor is defined by its width. The gain factor, β is proportional to the width of the transistor (p-transistor for a low-to-high transition and n-transistor for a high-to-low transition), W, and the mobility of the carrier (μ_p for low-to-high, μ_n for high-to-low). Hence,

$$P_{sc} = k\mu W\tau \quad (3)$$

where $k = c\frac{(V-2V_T)^3}{12T}$, c is a constant of proportionality. It is clear from equation 3 that the short circuit power consumption is directly proportional to both the width of the transistors and the input transition time.

Let us look at the case where a given CMOS gate is driving a load of several other CMOS gates. Consider

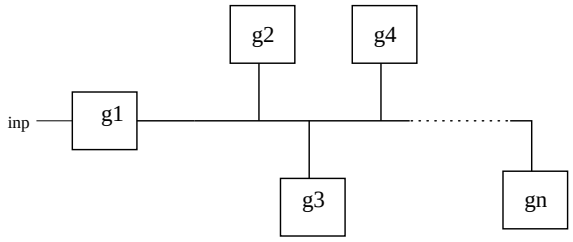

Figure 1: High fanout gate

the circuit of figure 1. Gate g_1 is driving $g_2, g_3, .., g_n$. The width of the transistor of the gate g_1 is denoted by W_1 and its output signal has a transition time of τ_1. Let us assume, for simplicity that the widths of both the p-type and the n-type transistors of a gate are the same. We will remove this assumption later. The input signal transition time for the gates $g_2, g_3, .., g_n$ is τ_1, which is the output transition time of g_1. Let us assume that $W_2, W_3, ..., W_n$ denote the widths of the transistors of the gates $g_2, g_3, .., g_n$ respectively. The total power consumed by the circuit is given by:

$$P = V^2 \sum_{i=1}^{n}(C_{L_i} f_i) + k(W_1\mu\tau + \sum_{i=2}^{n} W_i\mu'\tau_1) \quad (4)$$

The first term in equation 4 is the total capacitive power consumption, which is little affected by the sizing of the gate g_1. The second term is the total short circuit power consumption in all the gates. Here τ is the input transition time applied to the gate g_1, μ is the mobility of the carrier responsible for the transition in g_1 and μ' is the mobility of the carrier responsible for the opposite transition in the gates $g_2, g_3, .., g_n$.

Based on the delay model developed by Hedenstierna and Jeppson [6] the output signal delay of an inverter is given by

$$\tau = \phi\frac{C_L}{\mu W} + \frac{1}{6}\tau(1 + \frac{2V_T}{V}) \quad (5)$$

the first term is the delay response to a step function based on the gate geometry and the second term is the delay due to the input transition time. Here C_L is the total load capacitance of g_1 and is proportional to $2\sum_{i=2}^{n} W_i$ (assuming $W_{i(p)} = W_{i(n)}$) and μ is the electron/hole mobility. $\phi_{(n/p)}$ is a process dependent constant.

Substituting τ_1 in equation 4 by equation 5 we get the following expression for the total power:

$$P = P_{cap} + k(W_1\mu\tau + \sum_{i=2}^{n} W_i\mu'(\phi\frac{2\sum_{i=2}^{n} W_i}{\mu W_1} + \frac{\tau}{6}(1 + \frac{2V_T}{V}))) \quad (6)$$

simplifying,

$$P = P_{cap} + kW_1\mu\tau + k\phi\mu'\frac{2(\sum_{i=2}^{n} W_i)^2}{\mu W_1} + kk_2\sum_{i=2}^{n} W_i\mu'\tau \quad (7)$$

The right hand side of equation 7 has the form $\alpha * W_1 + \frac{\sigma}{W_1} + \delta$.

We performed SPICE simulations using 1.2 micron HP process parameters to compute the total power consumption of a circuit consisting of an inverter driving five uniformly sized inverters with 4λ wide transistors as load. The inputs to the driving inverter is derived from another fixed sized 'driver' and the output of each of the load inverters are connected to a capacitive load of 5pF to simulate an actual circuit scenario. The average power consumption of the circuit for the rising and falling transitions is plotted when we sized the p-transistor of the gate from minimum-size (3λ) and up, keeping the n-transistor at the minimum size. We selected three random points from the experimental results to compute the coefficients for equation 7 and plotted the curve against the results obtained from SPICE simulation in figure 2. Our model for power consumption matches the experimental results very closely.

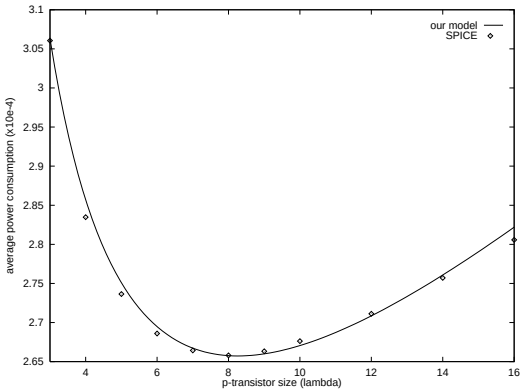

Figure 2: Comparison of our model with SPICE results

Note that the curve represented by equation 7 is convex i.e., it attains a global minimum for a certain value of W_1. W_1^*, the width of the transistor in g_1 that minimizes P is given by,

$$W_1^* = \frac{\sqrt{2\phi(\mu'/\mu)}(\sum_{i=2}^{n} W_i)}{\sqrt{\mu\tau}} \quad (8)$$

The power optimal p-transistor size is given by substituting μ_p, the hole mobility for μ, μ_n for μ', and ϕ_p for ϕ in equation 8 and the power optimal n-transistor size can be obtained by substituting μ_n, μ_p and ϕ_n respectively.

The W_i's in the summation of equation 4 are assumed to be equal for both the n-transistor and the p-transistor. In practice, for the rising transition in gate g_1, W_1 is the width of the p-transistor in g_1 and the W_i's are the n-type transistors in the gates $g_2, g_3, .., g_n$. The opposite

holds for the falling transition. Usually the $W_{i(p)}$'s are larger than the $W_{i(n)}$'s. Let us also include the interconnect capacitance, C_I in the load capacitance. Hence,

$$W^*_{1(p)} = \frac{\sqrt{\phi_{(p)}\mu_n(\sum_{i=2}^{n} W_i + C_I)(\sum_{i=2}^{n} W_{i(n)})}}{\mu_p\sqrt{\tau}} \quad (9)$$

$$W^*_{1(n)} = \frac{\sqrt{\phi_{(n)}\mu_p(\sum_{i=2}^{n} W_i + C_I)(\sum_{i=2}^{n} W_{i(p)})}}{\mu_n\sqrt{\tau}} \quad (10)$$

Equations 9 and 10 give the power optimal size for the transistors in a gate driving a given load. The power optimal size varies linearly with the size of the load driven by the gate. The power optimal size varies inversely with the square root of the input transition time, i.e., power optimal sizes are larger for faster input transitions. Since $\mu_n \sim 2\mu_p$, the effect of μ and μ' in equation 8 together implies that the power optimal p-transistor size is about $2^{3/2}$ times greater than that for the corresponding n-transistor. SPICE simulations were done using 1.2μ technology and varying the fanout load and input transition time for both rising and falling transitions. The results verify the above observations [2].

Table 1: Power optimal sizes and corresponding power savings (SPICE)

Fan-out	Pow-opt size p , n	Power reduction from min-sized
2	4λ , 3λ	1.39%
5	8λ , 4λ	15.57%
10	14λ , 6λ	35.35%
20	24λ , 10λ	57.82%

We sized both the p-transistor and the n-transistor together to obtain the overall power optimal configuration for the circuit. Table 1 shows the results of sizing both the transistors together to the individual power optimal size for a circuit consisting of an inverter driving a variable fanout load. The power saving with power optimal sizing increases with the increase in the fan-out load of the gate.

2.2 Extension to general CMOS gates

So far we have considered only CMOS inverters for our analysis. However, for our model to be applicable to a general circuit we need to extend this model for a general CMOS gate. We consider the problem of power optimal sizing of series connected MOSFETs here. For simplicity, we assume that the inputs to the series structure arrive simultaneously and they are sized uniformly; however, reordering of inputs and tapering of the chain of transistors is required for power optimization.

Several researchers proposed extension of the inverter based delay model for series connected MOSFETS [13, 14, 3]. The problem is commonly framed as that of finding the equivalent width of a single inverter that would result in the same delay as the chain of MOSFETs. The authors of [13] also considered the power consumption of the gate. In simple terms the equivalent width of N-series connected transistors for the same delay as that of a single inverter with width W is approximately $N \times W$. Using this equivalent inverter model in the derivation of equation 8 we get the following expression for the power-optimal size of a gate with N series connected MOSFETs in terms of the power optimal size for an inverter with the same load:

$$W_N = NW_1 \quad (11)$$

where W_N is the power optimal width of a series of N MOSFETS and W_1 is the power optimal size of an inverter. Using 1.2 micron technology, the results for a two and three input NOR gates are compared with that of an inverter in figure 3.

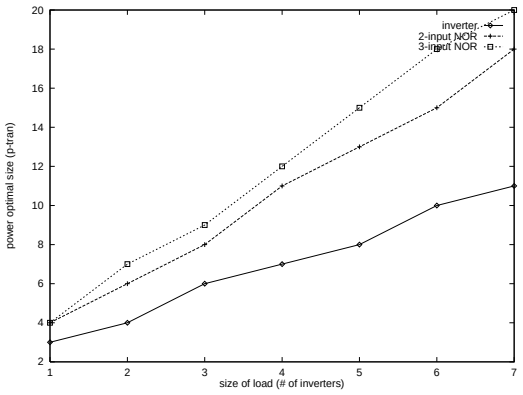

Figure 3: Power optimal sizes for NOR gates compared to that of inverter

2.3 Power-delay product

Let us consider the circuit of figure 1 again. The delay of the gate $g1$ is affected by increasing the size of the transistor. It is apparent from equation 5 that the delay of the circuit decreases with increase in the transistor size. The power-delay product with transistor sizing is given by equation 12 which, when simplified with respect to W_1 is of the form shown in equation 13.

$$PD = \left[P_1 + kW_1\mu\tau + k\phi\mu'\frac{2(\sum_{i=2}^{n} W_i)^2}{\mu W_1}\right]\left(\frac{\phi C_L}{\mu W_1} + k_2 t_{in}\right) \quad (12)$$

$$PD = A + B * W_1 + \frac{C}{W_1} + \frac{D}{W_1^2} \quad (13)$$

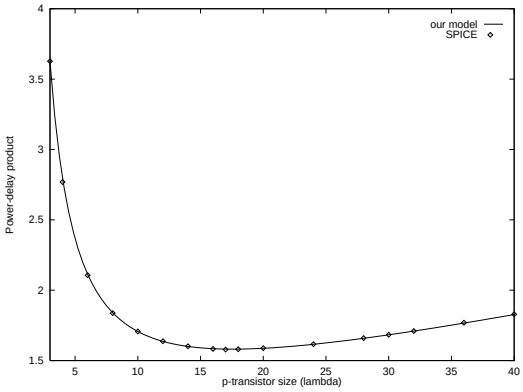

Figure 4: Comparison of our power-delay model with SPICE

We computed the coefficient in equation 13 using four sample points from SPICE simulation results for an inverter with a load of five uniformly sized inverters. The predicted power-delay curve using our model is plotted against the actual power-delay curve obtained from SPICE simulation in figure 4. The accuracy of our model with respect to SPICE results is apparent from the two curves.

The right hand side of equation 13 is a convex function of W_1 and attains a global minimum for certain W_1. The value of W_1 for which this function attains a minimum is the *power-delay optimal* size of the transistor for a given

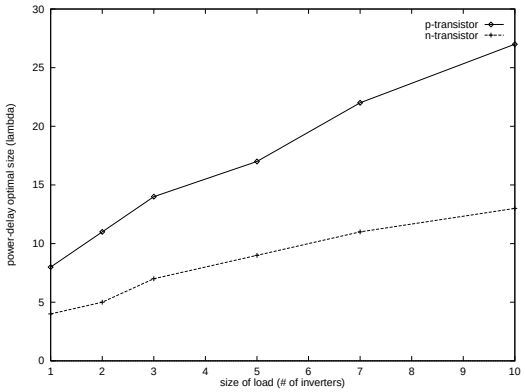

Figure 5: Variation of power-delay optimal size with load

load. The value of the power-delay optimal size of a transistor is much larger than the value of power optimal size for the same load. The variation of the power-delay optimal sizes for the p and n-transistor with various load sizes, as obtained from SPICE simulations is shown in figure 5. The power-delay optimal sizes also vary linearly with load. Figure 6 shows the variation of the power-delay optimal size with different input transition times.

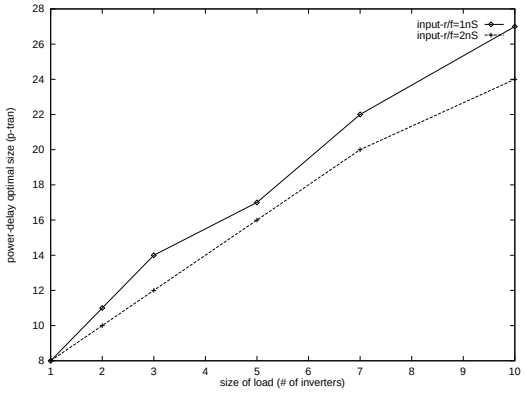

Figure 6: Variation of power-delay optimal size with input transition time (p-transistor)

The relation among the curves for delay(equation 5), power(equation 7) and power-delay(equation 13) are represented graphically in figure 7. When the size of the transistor is below the power optimal size, the power and delay both decrease with an increase in the transistor size. As a result the power-delay product decreases very fast (region A of figure 7). Beyond the power optimal size the power consumption starts to increase with the increase in transistor size while the delay of the gate still keeps decreasing resulting in a slower decrease in the power-delay product (region B), and reaches the power-delay optimal size. Beyond this size the power-delay product starts increasing (region C) because the rate of increase in power becomes more than the rate of decrease in delay.

Let us analyze the implication of the three regions in figure 7 with regards to a transistor sizing heuristic. When the transistors are in region A, we are in a win-win situation in terms of power and delay. Therefore, *all* transistors should be sized to at least up to the power optimal size. In region B, the reduction in delay is more than the increase in power. Therefore, we can profitably size a transistor in region B. The steeper the curve in region B, the more profit we get by sizing the transistor up.

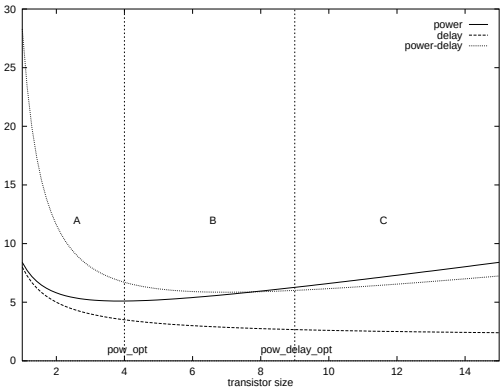

Figure 7: Sample curves for power, delay and power-delay

However, if the transistor is in region C, then its yield in speed is less than the increase in power consumption. Hence, among the transistors along the critical paths, any transistor in region B should be given preference over a transistor in region C while sizing. On the other hand, if we need to reduce the size of a transistor in region B, we should choose the one with the slowest rate of decrease in the power-delay product, because that is lying on the least benefit curve.

When the demand on the speed is very aggressive, the speed improvement by sizing the transistors within region B may not suffice. When a transistor is in region C, the slope of the power delay curve determines the sizing effectiveness of the transistor, i.e., the slope of the power-delay curve tells the tradeoff between the power and delay while sizing the transistor. Given two transistors in region C, the transistor with a smaller power-delay slope should be given preference for sizing as compared to a transistor with a steeper power-delay slope.

3 Power-delay driven transistor sizing

Based on the above observations, we suggest the following transistor sizing heuristic for power minimization of a circuit under a given delay constraint.

3.1 Power-optimal initial sizing

We propose that *all* the transistors in a circuit should be sized to their power optimal sizes given by equations 9 and 10. This will give the *minimum power configuration* for the layout with respect to transistor sizing, and any further sizing of transistors (enlarging or reducing) would only increase the power consumption of the circuit. This strategy may be applied as the initial transistor sizing heuristic; the transistors in a critical path may be sized further for speed.

While a transistor in a gate is being sized to power optimal size, the increase in its size is reflected in the load seen by the gate in the previous stage. The power optimal size of the gates in the previous stage are determined by the sizing at the current stage. Thus, the power optimal sizing should be done in a breadth-first(BF) traversal order, starting with the gates generating the primary outputs. A simple algorithm for power optimal sizing is given in figure 8.

3.2 Power optimization under delay constraint

Our optimization method starts with a power minimal layout configuration and attempts to proceed along a power optimal path to meet the required delay based

```
Algorithm power_optimal_initial_sizing()
    compute_load();
    todo_list = [gates driving the primary outputs];
    while (todo_list <> φ) do
        g = remove_head(todo_list);
        g.p_size = psizefunc(g,load);
        g.n_size = nsizefunc(g,load);
        flist = g.fan_in;
        for (f ∈ flist) do
            mark_visited(f,g);
            update_load(f,g);
            if (all gates in f.fan_out are visited) then
                todo_list = todo_list + [f] ;
        end (for loop)
    end (while loop)
```

Figure 8: The breadth-first algorithm for power optimal sizing

on the power-delay characterization in equation 12. The basic algorithm is given in figure 9.

The initial transistor sizing is performed using the power optimal transistor sizing algorithm given in figure 8. If the power minimal layout satisfies the required delay, we have produced a layout with minimum power consumption and the algorithm returns. The algorithm, after detecting the critical paths using a technique similar to PERT [12], size the transistors on the critical path to their power-delay optimal sizes (pd_optimal_size()), from the gates driving primary outputs towards the primary inputs, reflecting the change in the load capacitance due to increase in transistor sizes. If a transistor on the critical path is already sized beyond the power-delay optimal size (because it belongs to another critical path), it is left unchanged. The delay obtained in this configuration may be smaller than the requirement. If that is the case, then we have to reduce the size for some of the transistors along the path to reduce the power dissipation. The transistors which have the slowest slope on the power-delay curve are chosen for this purpose – the reason being that in this way we reduce the size of the transistors that were least profitable in power-delay product.

If the delay of the power-delay optimal layout is still more than the requirement, we have to size some of the critical path transistors further. The transistors with the least slope on the power-delay curve are considered for further sizing. Once again, the reason being that the transistors with steeper power-delay slope consume relatively more power for the same amount of delay reduction.

Algorithm power_optimal_initial_sizing() requires linear time on the number of transistors. The outer while loop in power-delay-opt() is executed only once for each critical path. Each iteration of the first inner while loop increases the size of one transistor by one unit while each iteration of the second inner while loop decreases the size by one unit. Computing the delays and critical path requires linear time on the number of transistors. Considering the worst case situation, the algorithm requires $O(N \times T)$ time, where N is the number of transistors in the circuit and T is the size of the largest transistor. In other words, the running time of the algorithm is proportional to the total active area of the layout.

4 Preliminary results

We implemented the power optimal transistor sizing heuristic based on equations 9 and 10 to perform initial transistor sizing for our in-house performance driven

```
Algorithm power-delay-opt()
begin
    perform power_optimal_initial_sizing();
    perform delay analysis and find critical path;
    while ∃ crit_path_delay > target + ε
        for each transistor ∈ crit_path
            if (size < pd_optimal size)
                size=pd_optimal size();
        end-for;
        compute delay along crit_path;
        if crit_path delay > target + ε
            /* increase transistor size */
            while crit_path_delay > target + ε
                find transistor with minimum
                    power-delay slope;
                increase size by one unit;
            end-while;
        else if crit_path_delay < target - ε
            /* decrease transistor size */
            while crit_path_delay < target - ε
                find transistor with minimum
                    power-delay slope;
                decrease size by one unit;
            end-while;
        end-if;
        recompute delays and find crit_path;
    end-while;
end;
```

Figure 9: Main algorithm for transistor sizing to optimize power under a delay constraint

module generator, Perflex[8], which uses transistor sizing and input reordering to generate high performance layouts. We selected a few arithmetic circuits to test our power optimal transistor sizing heuristic. The primary outputs of the circuit is assumed to have only one extra fan-out gate in the next module, similarly, the primary inputs are assumed to drive only one gate in the circuit. Therefore, the primary inputs driving more than one gate are derived from buffers which are subjected to power optimal sizing.

The layouts were first generated with all the transistors maintained at their minimum width (3λ) and the average power consumption for 100 random uniform input patterns were computed using SPICE. Next, all the transistors in the high fan-out gates were sized to their corresponding power optimal sizes using our heuristic. The same inputs were used to compute the average power consumption of the power optimal layout. Table 2

Table 2: The effect of power optimal transistor sizing on the test circuits

Circuit name	# transistors	% gates sized	Max tran. width (p,n)	Power saving compared to min-wid
SDA3	320	23	14λ , 7λ	15.3%
HALU	280	15	9λ , 4λ	5%
CLA4	244	19	10λ , 5λ	5.2%

presents the power saving obtained for each of the circuits. Note that SDA3, which has high percent of high-fanout gates (about 20%) produced a significant saving (more than 15%) in overall power consumption. HALU and CLA4, with fewer high fan-out gates represented a smaller saving.

Next, we considered the power optimization subjected to delay constraint. Work is in progress for developing an automatic layout tool for our heuristic. Presently,

we have used the power-delay optimal sizes from SPICE simulations at various loads to manually size the transistors in the critical path. We used an 8-bit and a 16-bit ripple carry adder (RCA) for this experiment. First, we generated the layouts for the circuits using only minimum-sized transistors and computed the power consumption and the critical path delay. Then we sized all the transistors along the critical path to their corresponding power-delay optimal sizes by hand. The power consumption and critical path delay of the circuit were computed using SPICE simulations.

Table 3: Power optimization subject to delay constraint

method used	avg. power (mW)	critical delay(nS)	power-delay product
8-bit RCA			
min-sized	0.9596	15.385	14.769
pow-dly opt	1.0045	10.831	10.879
16-bit RCA			
min-sized	1.4435	32.106	46.345
pow-dly opt	1.5673	24.421	38.275

The results of the experiment are shown in table 3. The second column presents the average power consumption for 100 random input patterns (30nS cycle time for RCA-8 and 40nS for RCA-16) and the third column represents the worst case delay through the circuit. The power-delay optimal sizing resulted in a much smaller power-delay product for both the circuits as compared to the minimum-sized gates. This initial experiment illustrates that the overall power-delay product of a circuit can be minimized by minimizing the power-delay product of the individual gates using our heuristics. Thus, using our power-delay optimization based transistor sizing heuristic it is possible to meet the delay requirement with minimal power consumption.

5 Conclusions

We formulated the problem of transistor sizing for minimizing the power consumption of a circuit under delay constraint. Based on accurate analysis of short circuit power consumption and gate delay in a sub-circuit containing drivers and loads together, we obtained power optimal transistor sizes and hence the minimum power configuration for a layout with respect to transistor sizing. The analysis of power-delay product of a gate in combination with the load devices led us to a new approach for computing the transistor sizes to minimize the power consumption of a circuit meeting the given delay requirement. The preliminary results from real circuits are encouraging. The authors are presently developing a module generator to perform transistor sizing for minimizing power consumption of a circuit subject to delay constraint automatically.

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