Revision part 3 for CNG3430 (version 7a)

1. An embedded system board obtains its power from a perfect voltage source of 5Volts via a 15-inch power cable of inductance 10nH per inch. The board has 300 gates, each has a load capacitance of 10pF. The allowable voltage drop anywhere inside the system is 0.3Volts. The shortest rise time of the signals is 5ns.

The system has three identical board level bypass capacitors connected in parallel (each capacitor has a value of C2 and a series inductance of 5nH) for supplying current to the board.

Also, the system has a capacitor array of N capacitors for disturbing current to the components. Each element of the capacitor array has a value C3 and a series inductance of 5nH. State any assumptions you used in the calculations.

* 1. Calculate the minimum value of C2.
  2. Calculate the minimum values of N and C3.
  3. If the three bypass capacitors are removed from the board, recalculate the minimum values of N and C3.

ANSWER:

1. I=NC dv/dt=300\*10p\*5V/5ns=300\*10\*(10^-12)\*5/(5\*10^-9) =3A

Noise level allowed=0.3V=E

Xmax=E/I=0.3V/3A=0.1 Ohms

C2\_tot=2\*C2, total capacitance of the two C2s in parallel

At Freq F1, inductance of L1 is the same as C2\_tot = 0.1 Ohms

Xmax=0.1 ohms = 2\*pi\*F1\*L1, L1=150nH=power cable inductance (15 inches , 10nH per inch)

So F1=0.1/(2\*pi\*150nH)= 0.1/(2\*pi\*150\*(10^-9)),

F1=1.0610e+005=106.1KHz=106100

AT F1 again, 1/(2\*pi\*F1\*C2\_tot)=0.1 Ohms

C2\_tot=1/(2\*pi\*F1\* (0.1Ohms))= 1/(2\*pi\*106100\*0.1)= 1/(2\*pi\*106100\*0.1)= 1.5000e-005

**So C2\_tot=1.5000e-005/(10^-6)= 15uF,**

**each C2 is (15/3)uF=5uF**

1. At tr=5ns edge, the knee frequency is 0.5/tr=0.5/5ns=100MHz

The capacitor array (each has 5nH series inductance) has N elements and total inductance is L3\_tot=5nH/N))

It should not block 100Mhz, so 2\*pi\*100MHz\*L3\_tot=2\*pi\*100\*10^6\* L3\_tot =0.1 Ohms

L3\_tot=0.1/(2\*pi\*100\*10^6)= 1.5915e-010

L3\_tot= 1.5915e-010=5nH/N,

so N=>5nH/ L3\_tot =(5\*10^-9)/ 1.5915e-010=31.4169, so N=32

At F2 the capacitor array starts functioning,

2\*pi\*F2\*L2\_tot=0.1 Ohms , L2\_tot=5nH/3=1.667nH

F2=0.1 Ohms/(2\*pi\*1.667nH)= 0.1 /(2\*pi\*(1.667\*10^-9))

F2=9.5474e+006=9.55 Mhz

1/(2\*pi\*C3\_tot\*F2)=0.1 Ohms

C3\_tot=1/(2\*pi\*9.55Mhz\*0.1)= 1/(2\*pi\*(9.55\*10^6)\*0.1)= 1.6665e-007

C3\_tot=166.7 nF

Since N\*C3= C3\_tot=166.7 nF

So C3=166.7nF/32=5.89nF

**N=32, C3=5.21nF**

1. If the three bypass capacitors C2s are not used, N remained unchanged, since it is calculated from the 100MHz , Tr edge parameters. But at lower frequency, it has to deal with the impedance starting from frequency F1=106.1KHz (Not F2 since on board bypass capacitors are gone)

1/(2\*pi\*C3\_tot’\*F1)=0.1 Ohms

C3\_tot’=1/(2\*pi\*106.1KHz \*0.1)= 1/(2\*pi\*106.1\*10^3 \*0.1)= 1.5000e-005

C3\_tot’=15uF

N\*C3’=C3\_tot’

C3’=15uF/32

C3’=0.4688uF

**N’=32, C3=0.4688uF**

1. A digital circuit in a system has 100 gates. In each gate, the output is switching a load of 10pF and the output voltage is between 0 and 5 Volts. The power cable connecting the power supply of 5 Volts to the circuit has an inductance of 200nH. The rise time of the digital signal is 5 ns. A board level bypass capacitor is used to stabilize the power supply for the system. It is found that the minimum value of the board level bypass capacitor C is 100μF. And the inductance at the legs of the capacitor C is 5nH.
   1. Calculate the maximum current drawn by the circuit.
   2. Calculate the equivalent frequency of the switching signal that the power supply is unable to supply current to the circuit through the power cable.
   3. Calculate the maximum voltage drop allowable in the power cable.
   4. Explain why a capacitor array of small capacitors is also needed for this circuit. The calculation of the number and actual values of the capacitor array is not necessary.

Answer:

1. Current=N\*C\*dv/dt=100\*10pF\*5/5ns=100\*10\*(10^-12)\*5/(5\*10^-9)=1A

Since board bypass capacitor impedance and inductance impedance should be the same.

2\*pi\*F1\*L=1/(2\*pi\*F1\*C1), hence

F1=sqrt(1/(2\*pi\*L\*2\*pi\*C1))

L=200nH=2\*100\*(10^-9), C=100uF=100\*(10^-6)

F1=sqrt(1/(2\*pi\*200\*(10^-9)\*2\*pi\*100\*(10^-6)))= 3.5588e+004Hz=35588 Hz

(c ) Xr= the maximum voltage drop allowable in the power cable

AT F1 , Xr=2\*pi\*F1\*L=2\*pi\*35588\*200\*(10^-9)= 0.0447 ohms

X=I\*Xr=1A\*Xr,

Xr=Vx/1A

Vx=I\*Xr=1A\* 0.0447 Ohms=0.0447 Volts

d)

Because the legs of the board level bypass cap is blocking current, cap array is needed.

1. A transmission line has a characteristic impedance of 75 Ohms and 10 meters long. At time 0, an input voltage of 1 Volt enters the source end of the line. Describe what would happen to the signal inside the line after each of following cases, and there is no need to calculate the actual reflected voltage values and time delays etc. (Assume the line is lossless.)
   1. If the source impedance is 75 Ohms and the load impedance is 75 ohms.
   2. If the source impedance is 75 Ohms and the load impedance is 0 ohms.
   3. If the source impedance is 0 Ohms and the load impedance is 75 ohms.
   4. If the source impedance is 0 Ohms and the load impedance is 0 ohms.

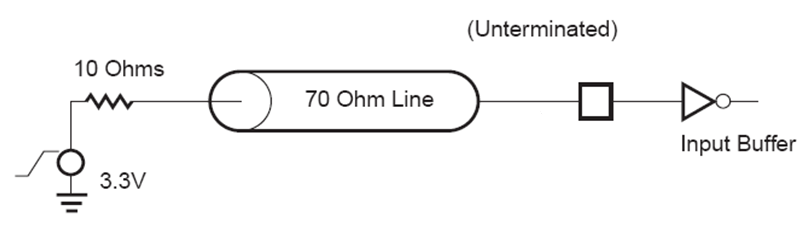
Answer:

1. no reflection
2. 100% reflection at load end, and reflected back, but halved at source end , and reflected back to the line . Finally it will reflect for some time and die down.
3. no reflection, all signals passed to the output
4. reflection forever assume no lost inside the line.

* A= Input acceptance func=Z0 /[Zs +Z0 ].
* T=Output transmission func.= 2ZL/[ZL+Z0]= 1+ R2
* R2=load-end reflective coef.=[ZL - Z0  ]/ [ZL + Z0 ]
* R1=source-end reflective coef.=[Zs - Z0 ]/[Zs + Z0 ]

1. An unterminated transmission line (open is an output circuit) is 1.5 inches and the line transfer characteristic P=1. The configure is shown below.

Calculate the voltage first reaches the output.



Answer: use the following formulas

* A= Input acceptance func=Z0 /[Zs +Z0 ].
* T=Output transmission func.= 2ZL/[ZL+Z0]= 1+ R2
* R2=load-end reflective coef.=[ZL - Z0  ]/ [ZL + Z0 ]
* R1=source-end reflective coef.=[Zs - Z0 ]/[Zs + Z0 ]

Vin\*A=3.3\*70/(10+70)=2.9V, P=1 so no attenuation inside the line, 2.0V reaches the output

ZL=un-terminated=∞, T=2ZL/[ZL+Z0 ]=2, So 2.9\*2=5.8V

