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Project Name: vgaChars

Creation Date: May 2003

Development Board: XESS XSA-100 Plus XStend Version 2

Development Software: Xilinx ISE Version 5.1.03i

Description

This project generates a vga signal and displays a set of characters generated from character ROM. The rom entity itself was generated using the Xilinx CORE Generator.

The XStend board is not needed in this project, except for the fact that I possibly still have some pin references to it.

The XSA-100 board frequency must be set to 25MHz!

Xilinx Core Generator

The core generator provides a nice interface to generate cores for Xilinx chips, duh! After starting a “project” (a place to store information related to building a new core) and answering a few questions a core is generated in the form of an EDIF file.

The core generator was used in this project to generate a character rom entity. Follow these steps to recreate the char_rom.edn file.

- 1) Open Core Generator (version 5.1.03i) and start a new project.
- 2) Set target architecture to Spartan 2 (this project is targeted at XSA-100 board). Also under “Design Entry” select “Exemplar”. Why? Because if you leave the setting at “ISE” you will most likely get an error. I found reference to this error on the Xilinx site, which claimed that it’s more of a warning, but I don’t get the EDIF file I need, so select Exemplar.
- 3) Select “Memories & Storage Elements”, and then select “RAMs & ROMs”.
- 4) Select a “Single Port Block Memory” (version 4). A dialog will open asking all sorts of questions.
- 5) Name the component. I call it “char_rom”. Set “Port Configuration” to “Read Only” and select “Memory Size” width to be 8 bits, by Depth of 512.

- 6) Click “Next>” twice to move to page 3. Nothing to do on page 2.
- 7) I selected the “Select Primitive” option and specified 512x8. This should use the Xilinx primitive for a Block Ram resource.
- 8) On the last page, page 4, click on “Load Init File” and select the charRomData.coe file. This file describes the initial contents of the block ram. It contains all the character data.
- 9) Click on “Generate” at the bottom of the page to create the char_rom.edn file to be included in your project. Just copy the file to the root directory location (the one with make.bat and clean.bat) so that it will be found.

Project Directory Structure

This project is organized into the following directories:

./ - contains all the files need to synthesize the design.

./core – contains .coe file used to initialize block ram contents during the specification on how to create the char_rom.edn (edif) file. Also contains the original source .mif (from an Altera project) file used as a starting point to build the .coe file. Basically, the original character ROM data is contained in charRomData – Altera.mif. After much editing in a text editor, the file called charRomData.coe file was created for the Xilinx core generator.

./config – effectively a backup of all main files in the root directory

./docs – this PDF file. Source files used to build this PDF are located in ./docs/src.

./src – source directory for all HDL files

./temp – temporary directory used during the build process.

Synthesis

The project is built and maintained using two windows based batch files. The first is “make.bat”. It simply issues are the commands required to “compile” all the source files in the ./src directory and eventually generate the chipIO.bit file to downloaded to the fpga.

The second batch file is called “clean.bat”. Its sole purpose is to delete most of the unwanted files generated during the build process.

References

Primary reference in building this project, specifically the vga signal generation circuit was the book titled “Rapid Prototyping of Digital Systems – A Tutorial Approach Second Edition”. I highly recommend this book for a collection of great design experiments!