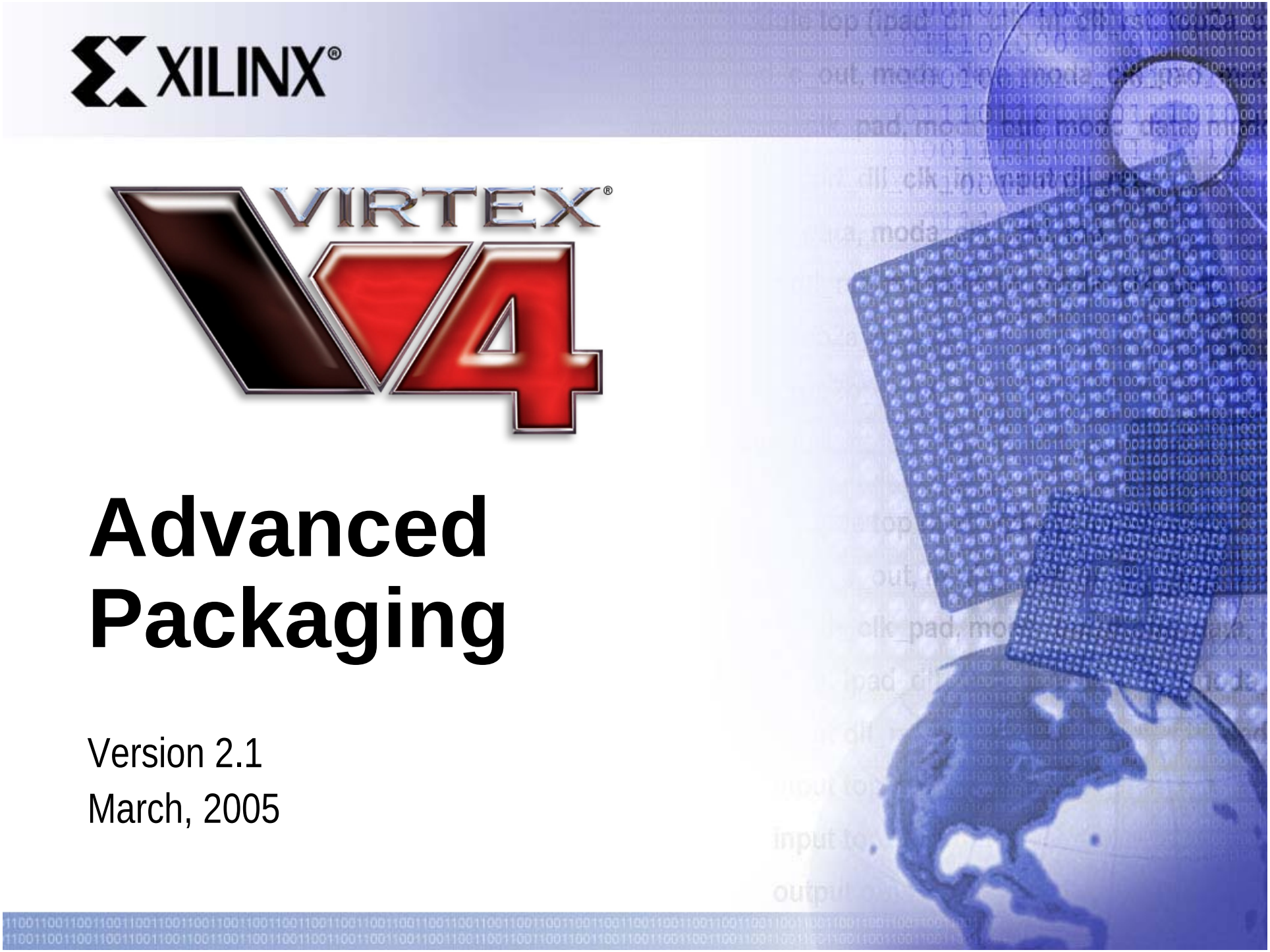


Advanced Packaging

Version 2.1

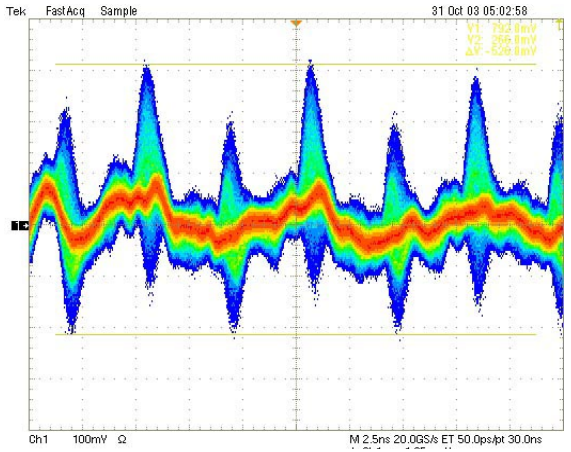
March, 2005

Agenda

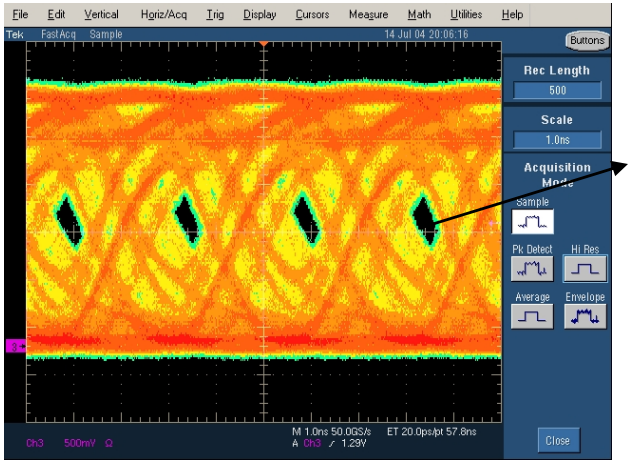
- Introduction
- Background
- Virtex-4 Solutions
- Summary

Packaging Impacts System Design

- Problem with high package inductance:
  - Voltage noise & GND bounce
  - Clock jitter & poor data eye
- Effect on System design:
  - Degrades system performance and sometimes system failure
  - Requires expensive and time consuming signal/power integrity analysis



Ground Bounce

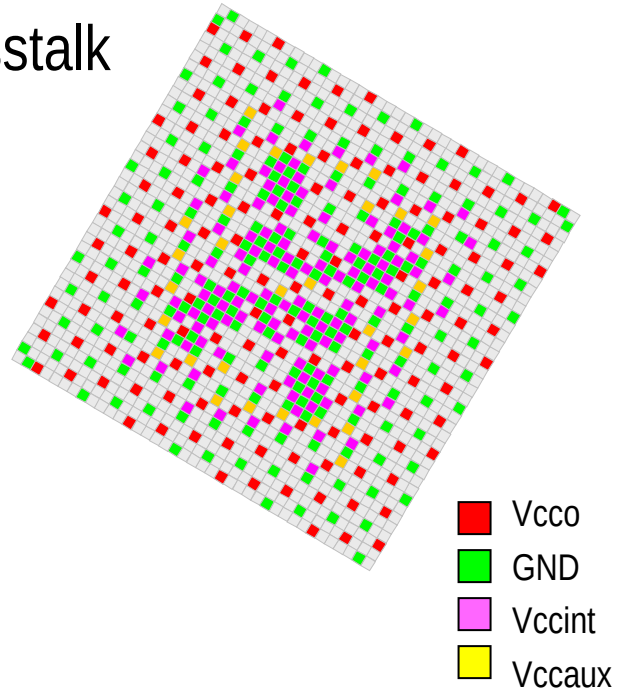


Poor Data Eye

Data Pin Eye Diagram

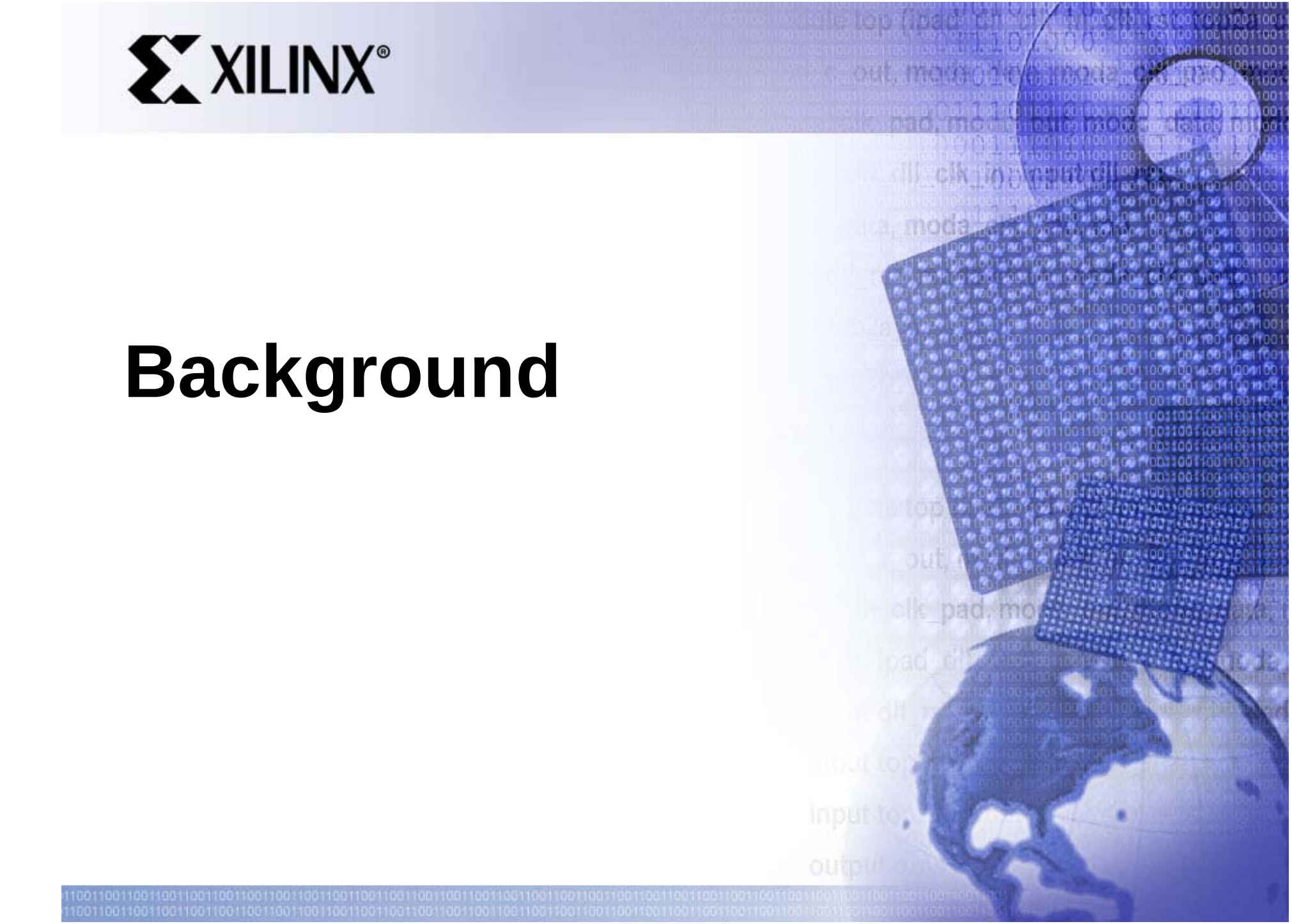
Virtex-4 Provides Advanced Packaging Solutions

- Improved signal, power integrity and crosstalk
  - Minimizes package & PCB inductances
  - More usable I/Os than competing solution
- Designed & verified with extensive simulation and hardware testing
- No additional PCB costs to customers
  - Use same number of PCB layers as previous generations



The Best Approach for High Pin-Count 90nm FPGAs

Background



When will Signal Integrity Be Critical

- Signal Integrity (SI) is crucial especially when
  - high-speed parallel interfaces in their system (e.g.,DDR/DDR2 memory interfaces).
  - high-speed or high slew rate signal is routed closely to each others
  - Tens or Hundreds of output switching at once

    (that is the so call “Simultaneous Switching Output ”)

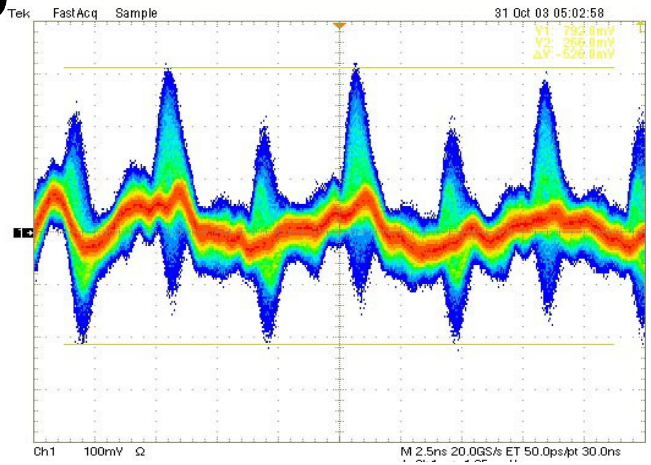
PCB Problem Areas

- Wide, high-speed single-ended IO interfaces (eg. 144-bit DDR 2 interface) often have signal and power integrity problems
- Packaging noise come from two major areas
  - Crosstalk impacts signal integrity
  - Inductance impacts power integrity
- Package & PCB via field crosstalk
  - Crosstalk between the package substrate vias, the package balls, and the PCB vias is the root cause
  - Locations of the Ground, power & IO pins determine the size of the return current path
  - Loop inductance L is proportional to the return current loop area
  - Crosstalk is proportional to loop inductance
- Primary cause for high inductance is contributed by substrate design and on-package capacitor
- Inductance impacts power integrity and cause clock jitter

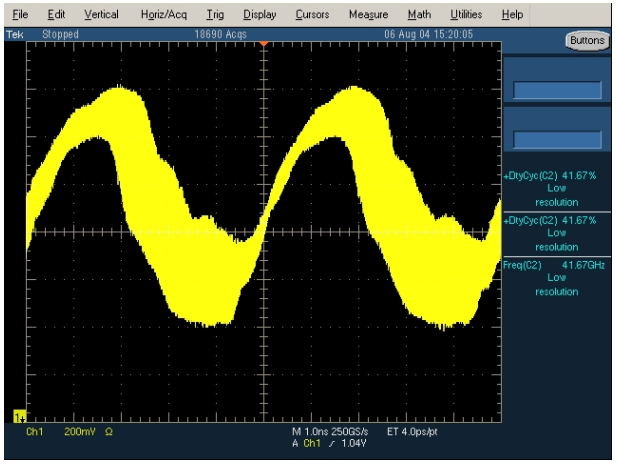
Packaging Impacts System Design

Pin-out & Packaging

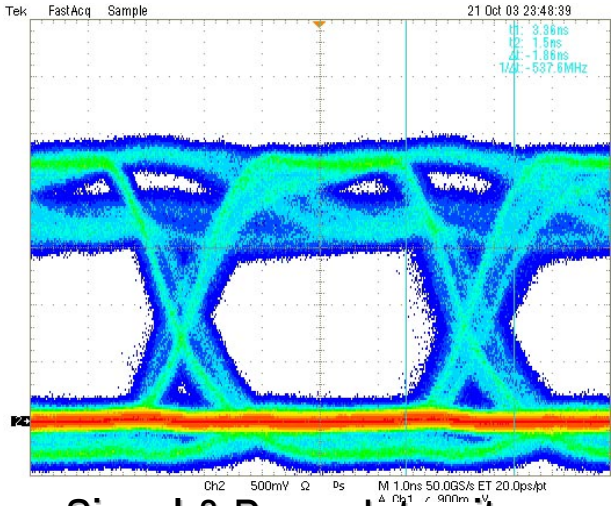
Package and PCB Inductance and Crosstalk



Ground Bounce/Voltage Collapse

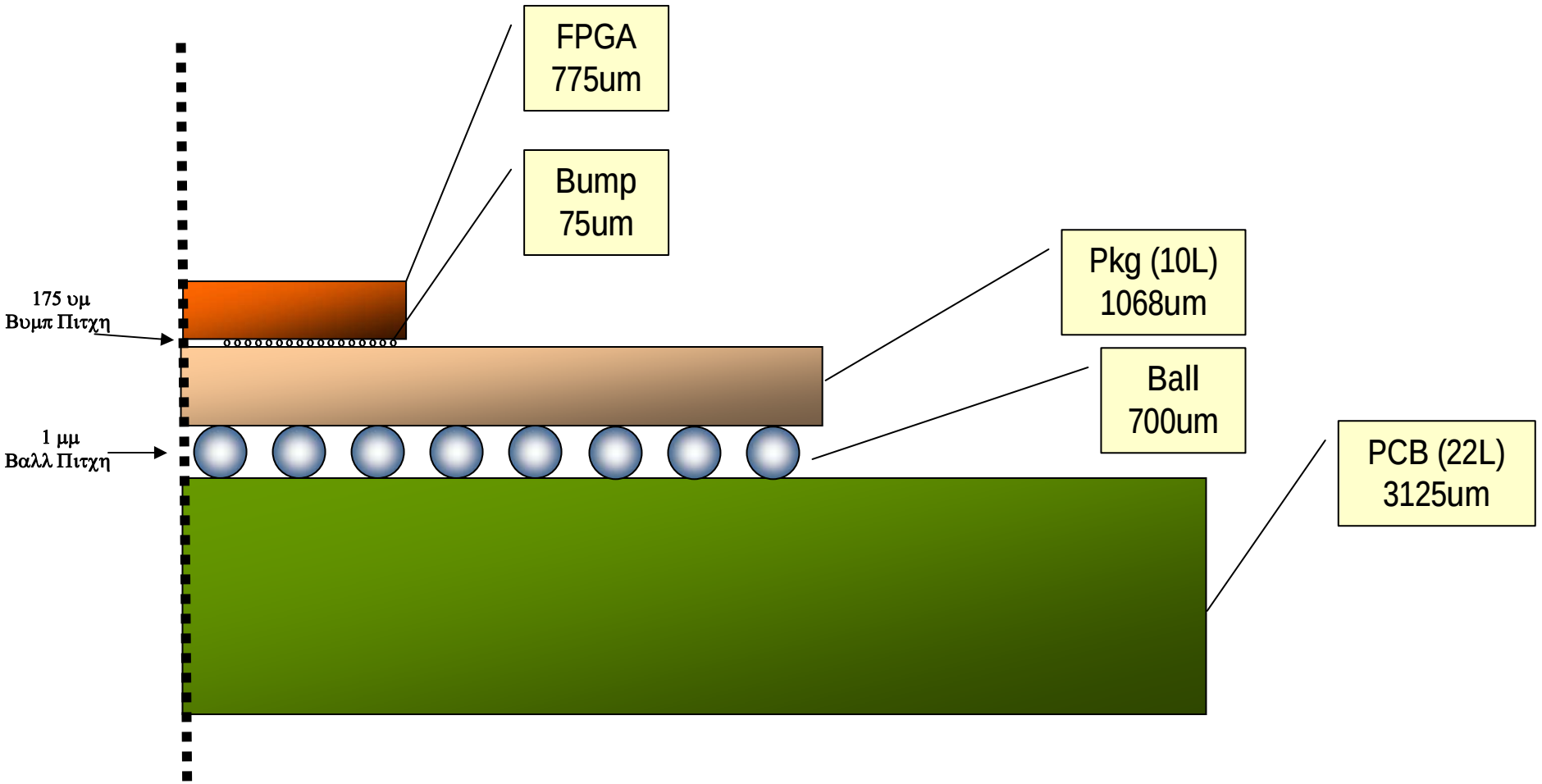


System Jitter

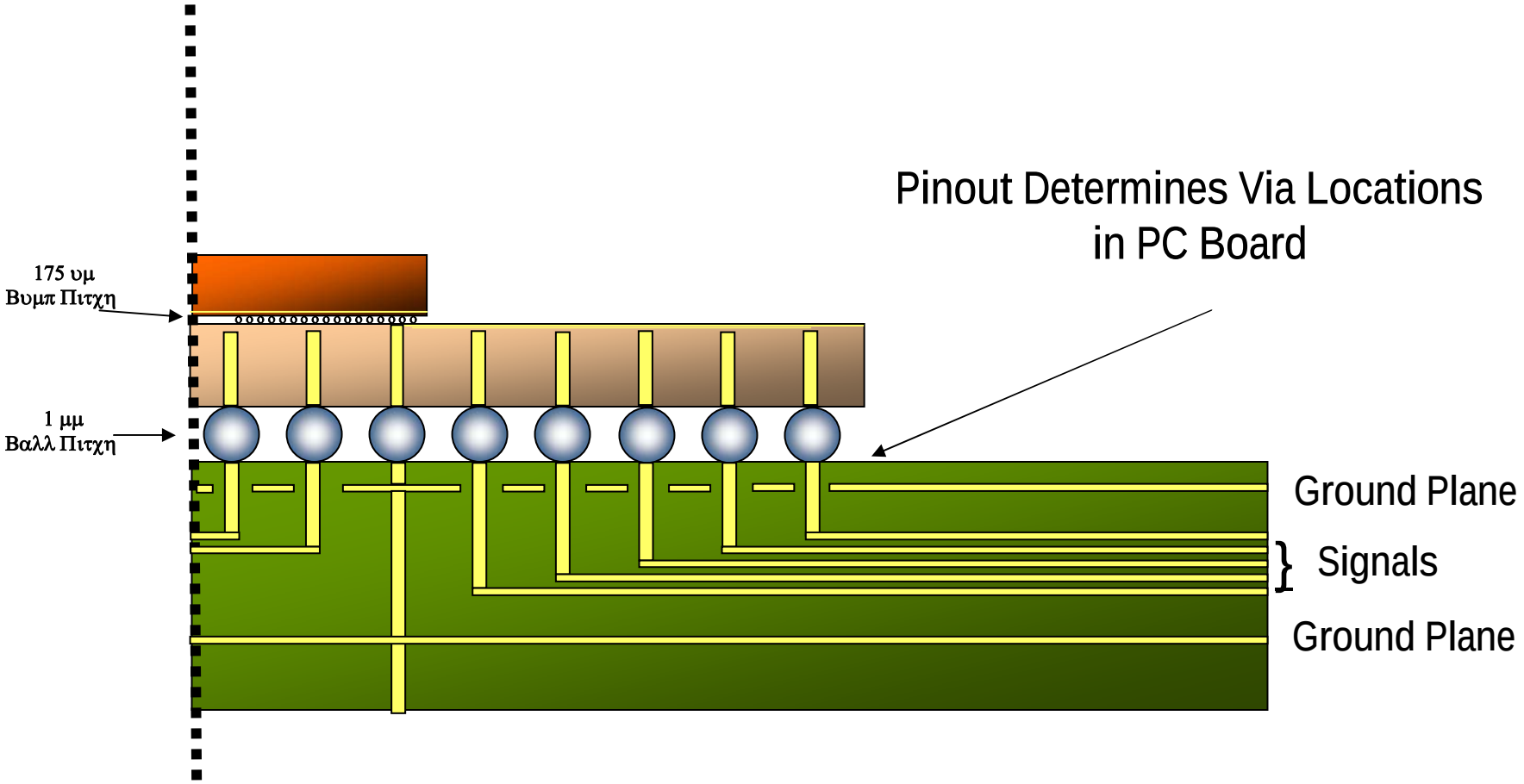


Signal & Power Integrity

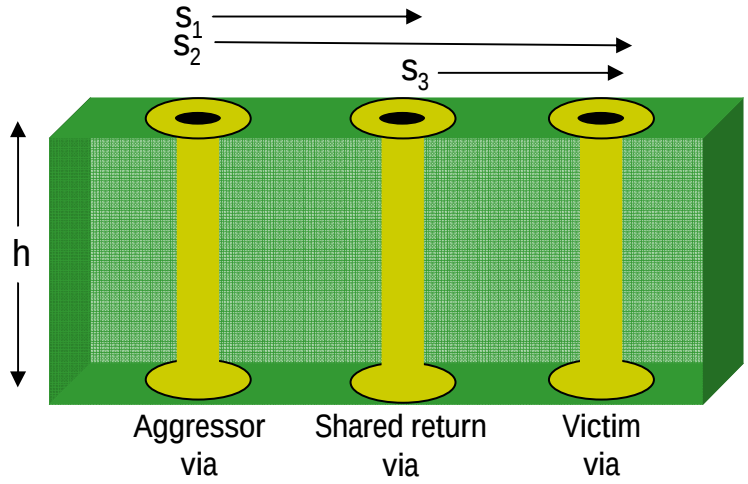
Die and Package Scale



Pinout Defines Via Fields



Via Crosstalk Formula



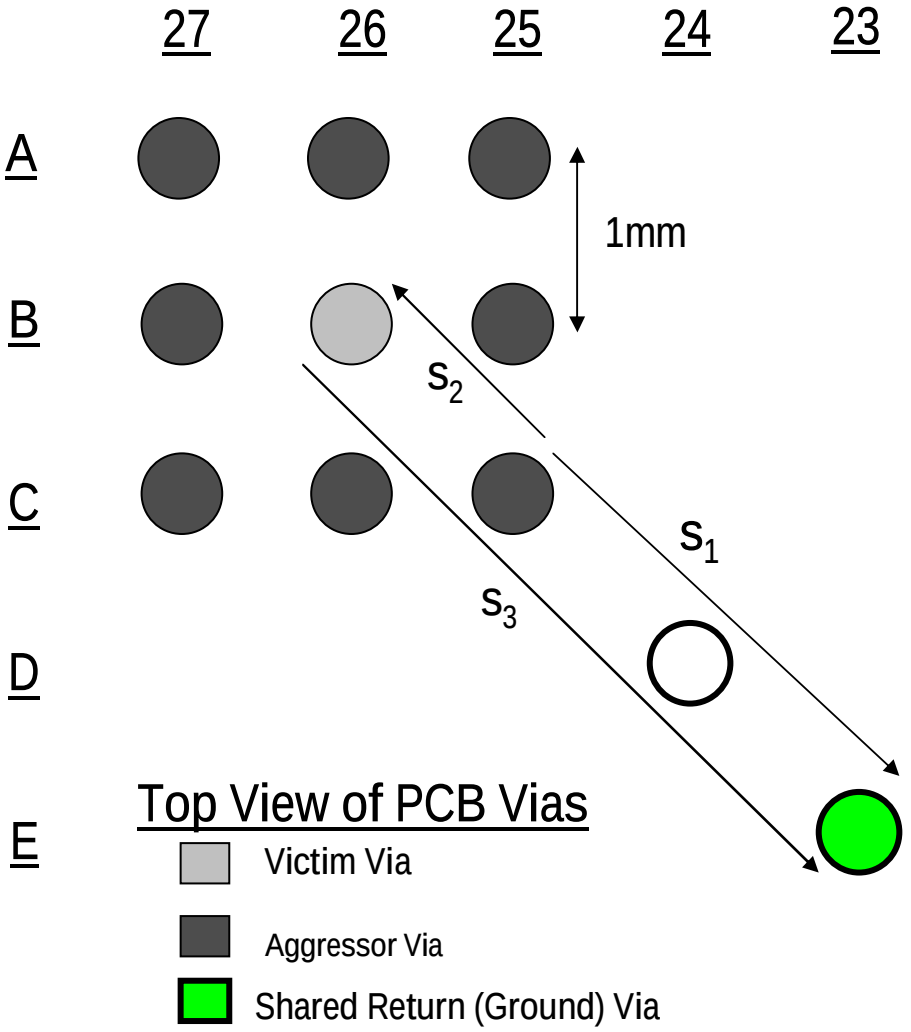
Vias in a PC Board

$$L_m = h \times 200 \times \ln(s_1 s_3 / s_2 r)\ \text{nH}$$

L_m is the mutual inductance between vias
h is the separation between the reference planes in the PC board (m)
s_1 is the horizontal distance from the signal via to the shared-return via (m)
s_2 is the horizontal distance from the signal via to the victim via (m)
s_3 is the horizontal distance from the shared-return via to the victim via (m)
r is the radius of the shared-return via (m)

Source: Pg 356-357, "High-Speed Signal Propagation"
Howard Johnson, Martin Graham

Traditional FPGA PCB Via Pattern



- Locations of the Ground, power & IO pins determine the size of the current loop
- Loop inductance L is proportional to the current loop area (A)

$$L = \mu_0 \frac{A}{w}$$

- Crosstalk is proportional to loop inductance

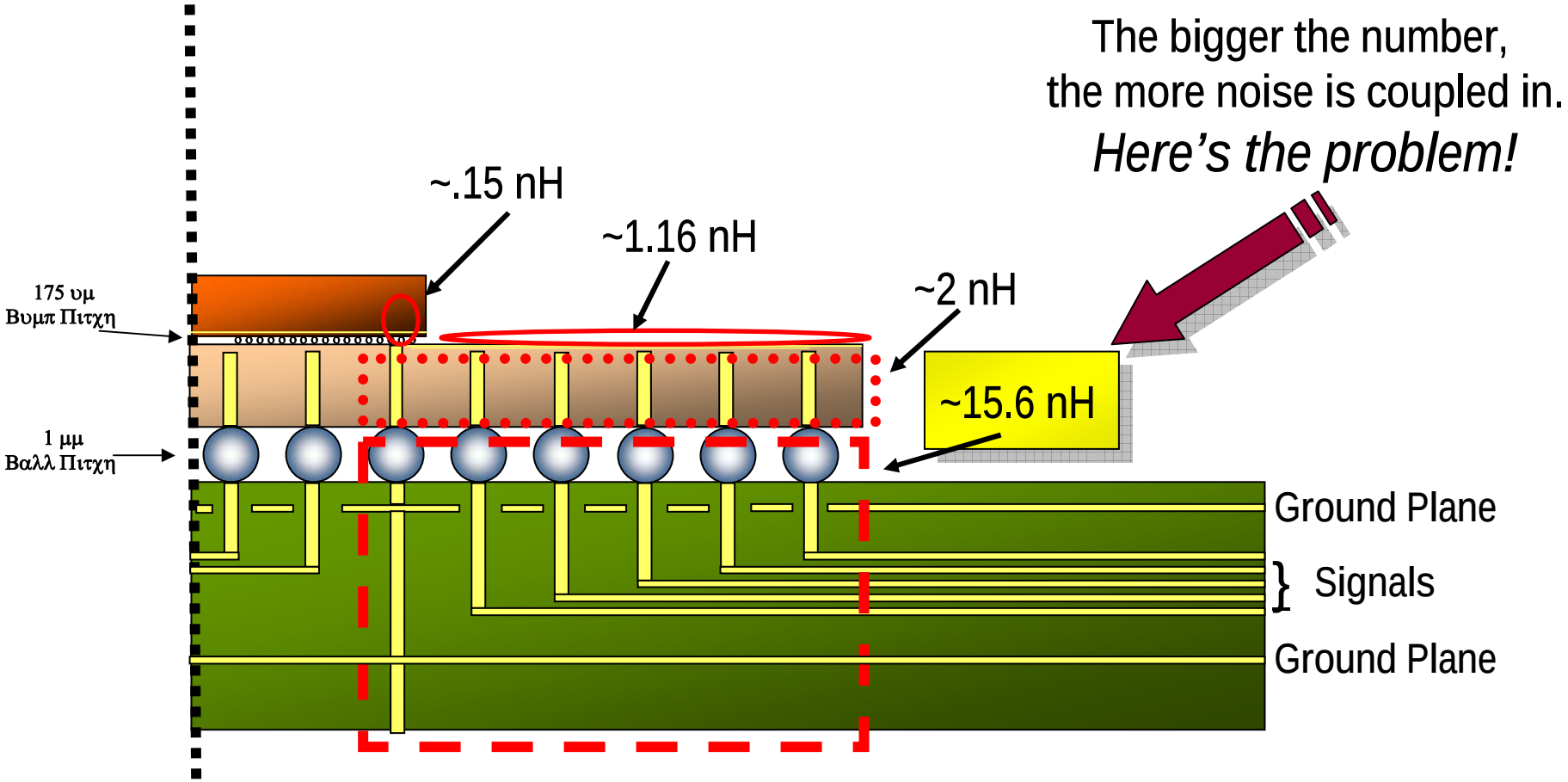
Examine aggressor via at C25 coupling into the victim via at B26:

$$L_m = h \cdot 200 \cdot \ln\left(\frac{S_1 S_3}{S_2 r}\right) nH$$

$$Noise = L_m \frac{di}{dt}$$

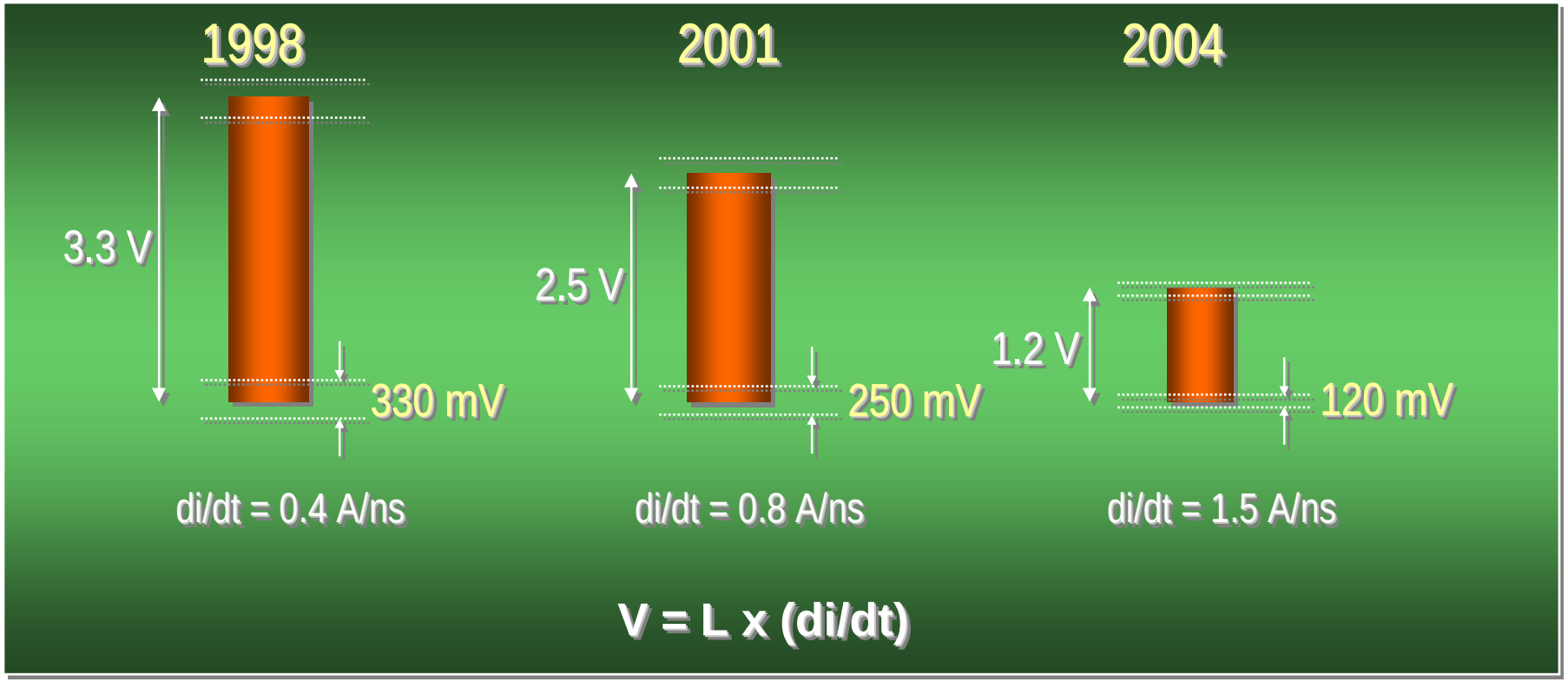
Total noise at victim via
= Sum of noise from all aggressor vias

Breakout of Total Mutual Inductance



82% of Noise is determined by the Pin-out and found in Package Balls and PCB vias

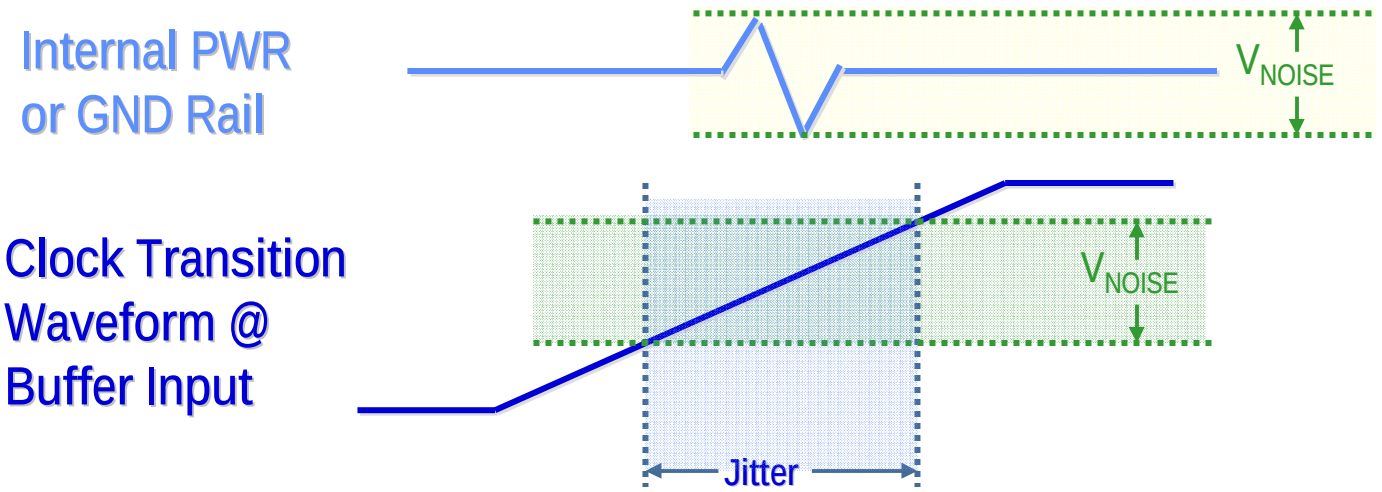
Maintaining Power Integrity



CMOS power supply noise tolerance remains constant over process generations at 10% of nominal

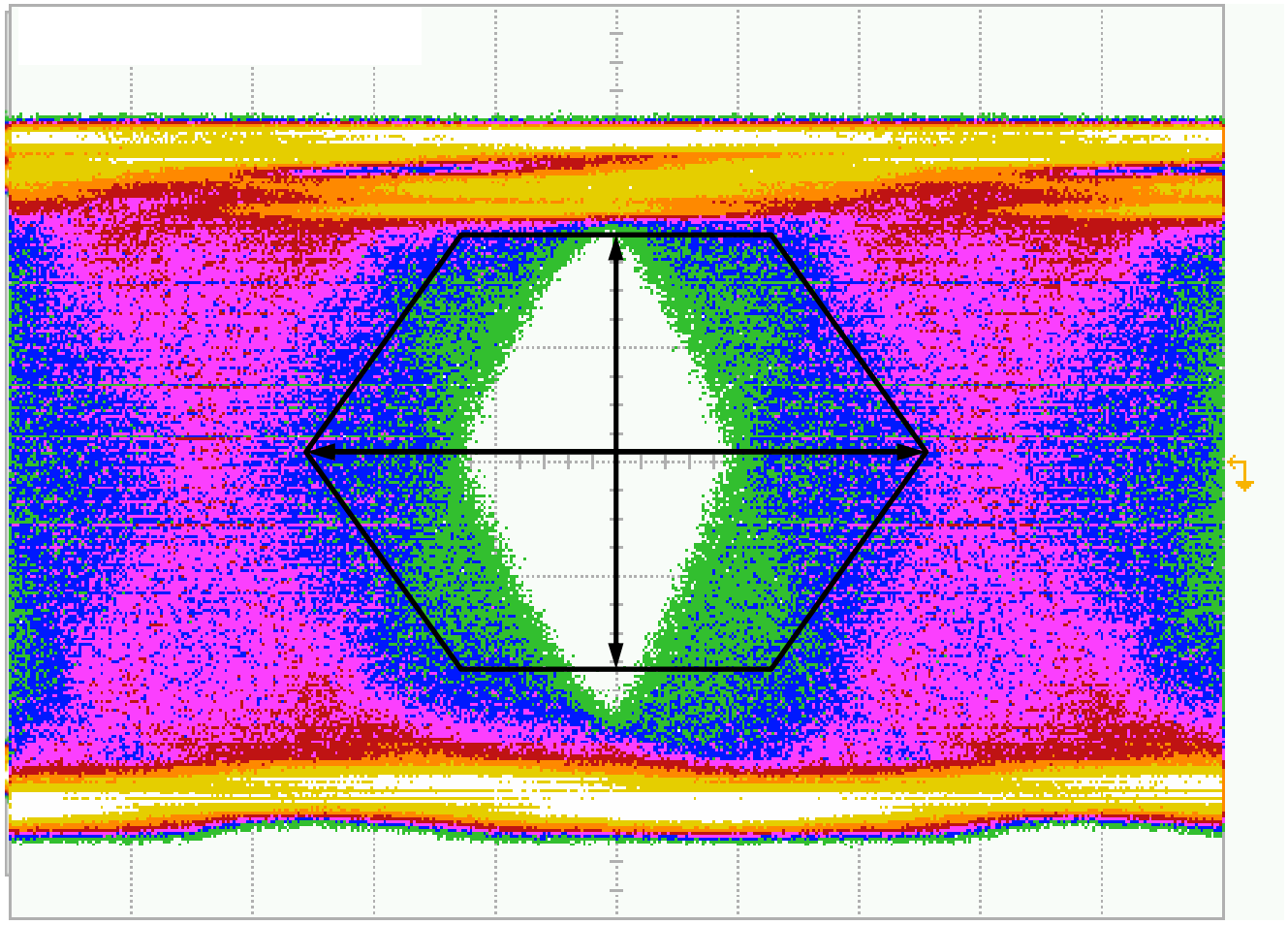
As di/dt Increases, Minimizing L is a Crucial Task to Meet the Tolerance Limit for the Supply Voltage

Voltage Noise Causes Jitter



- V_{NOISE} = Magnitude of the noise/ripple/GND bounce
- Jitter is directly proportional to the magnitude of the noise/ripple/GND bounce
- T_{JITTER} = dT/dV (of the clock) * V_{NOISE}
- Voltage noise at the die increases jitter, decreasing performance

Jitter Affects Overall Signal Integrity



Degrades System Performance & Reliability

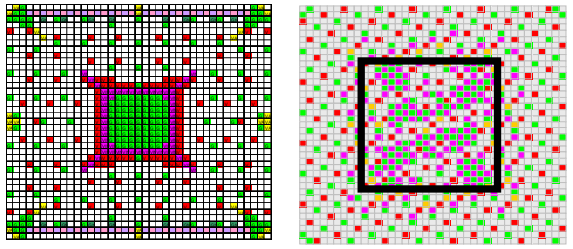
Virtex-4 Solution

Virtex-4 Advanced Packaging

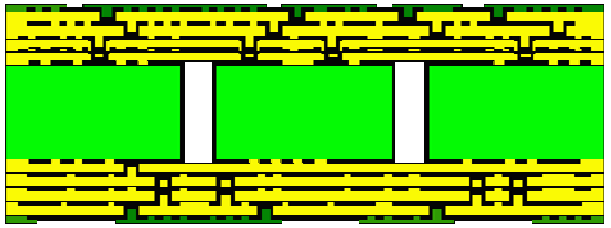
- Significant enhancements in package pin-out, on-package decoupling & substrate design
  - Improve I/O to Power/GND ratio
  - Offer solid V_{CCO} and GND references for signals
  - Provide multiple planes dedicated to Core and I/O power supplies
  - Deploy continuous Pwr/GND planes
  - Utilize very low inductance on-package decoupling capacitors
  - Increase substrate layer count from 6 to 10
  - Pay special attention to IO_CCLK, GCLK, Vrefs
- Unique SparseChevron™ pin-out addresses critical via crosstalk issue
- Advantages fully verified on Hardware platform and validated by industry SI expert

Virtex-4 Advanced Packaging Three major improvements

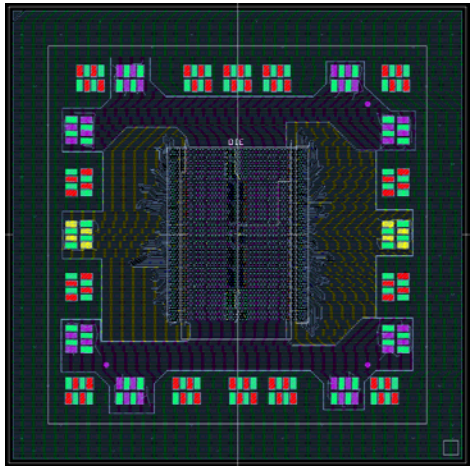
- Pinout Architecture



- Power plane integrity

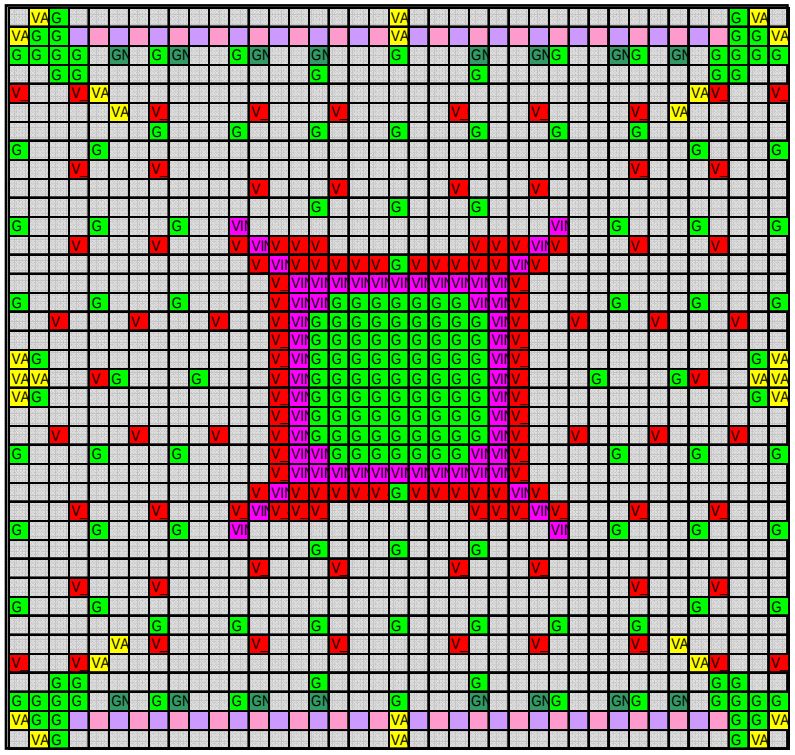


- Low-inductance capacitance

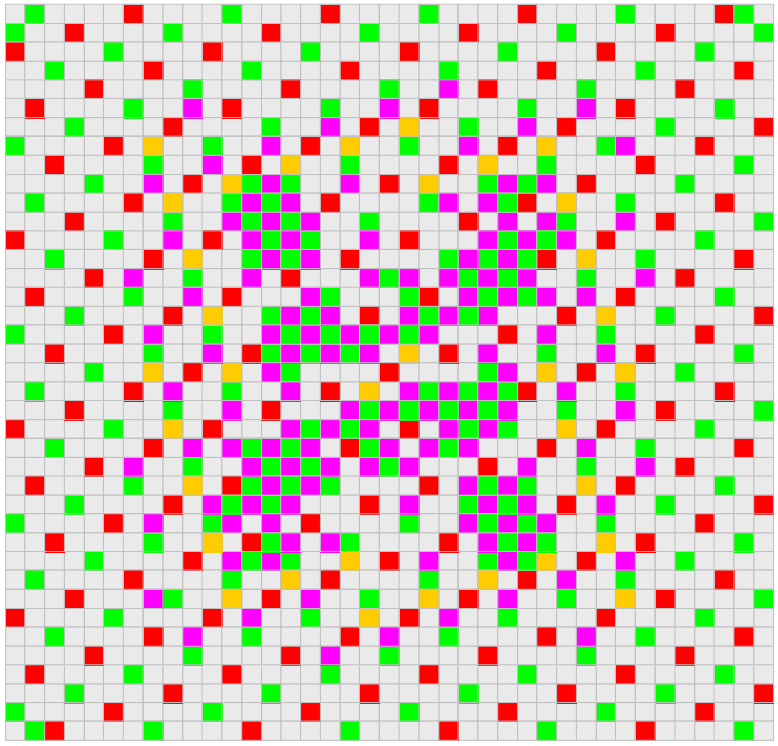


Virtex™-4 State-of-the-Art Packaging

Traditional SparseChevron™

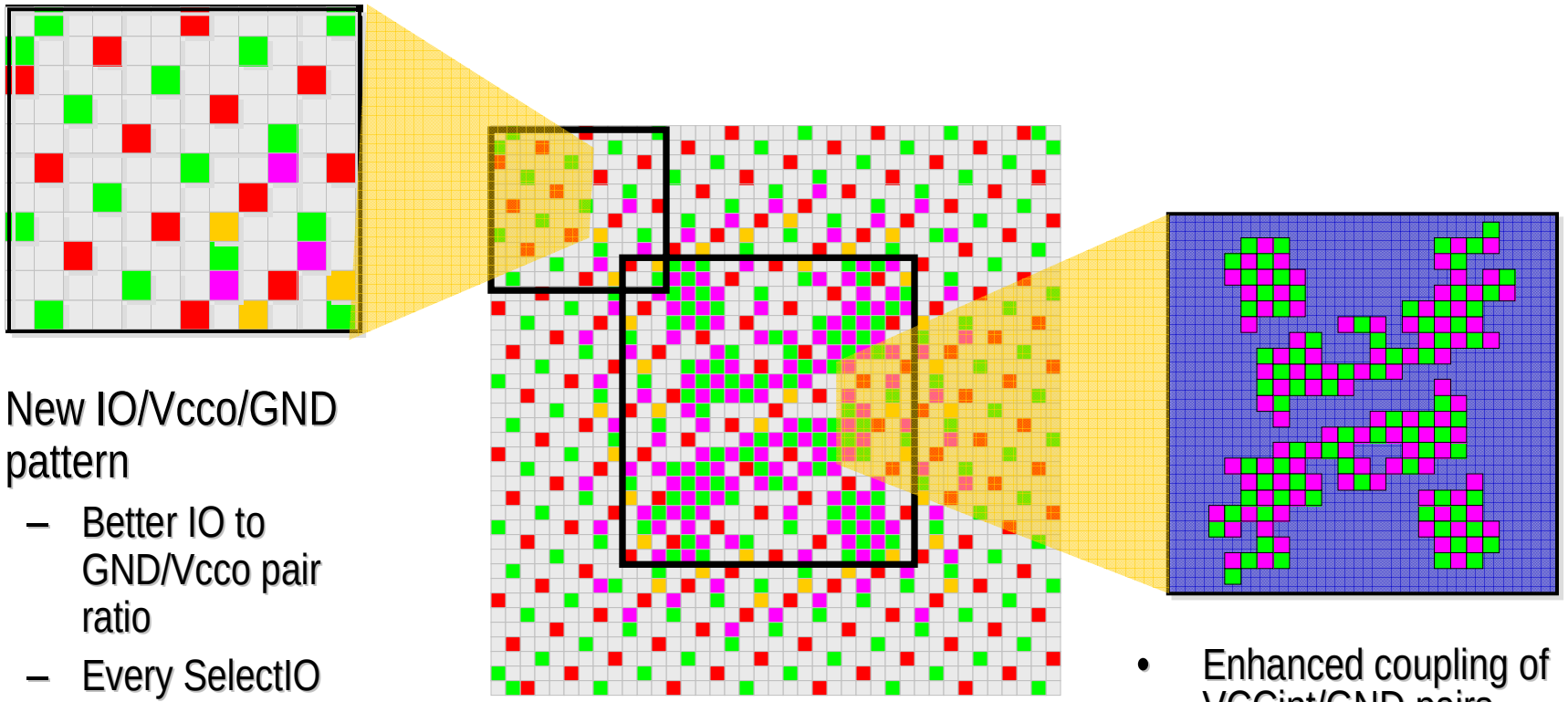


Virtex-II Pro FF1517 Package



Virtex-4 FF1513 Package

New Virtex-4 Advanced Packaging

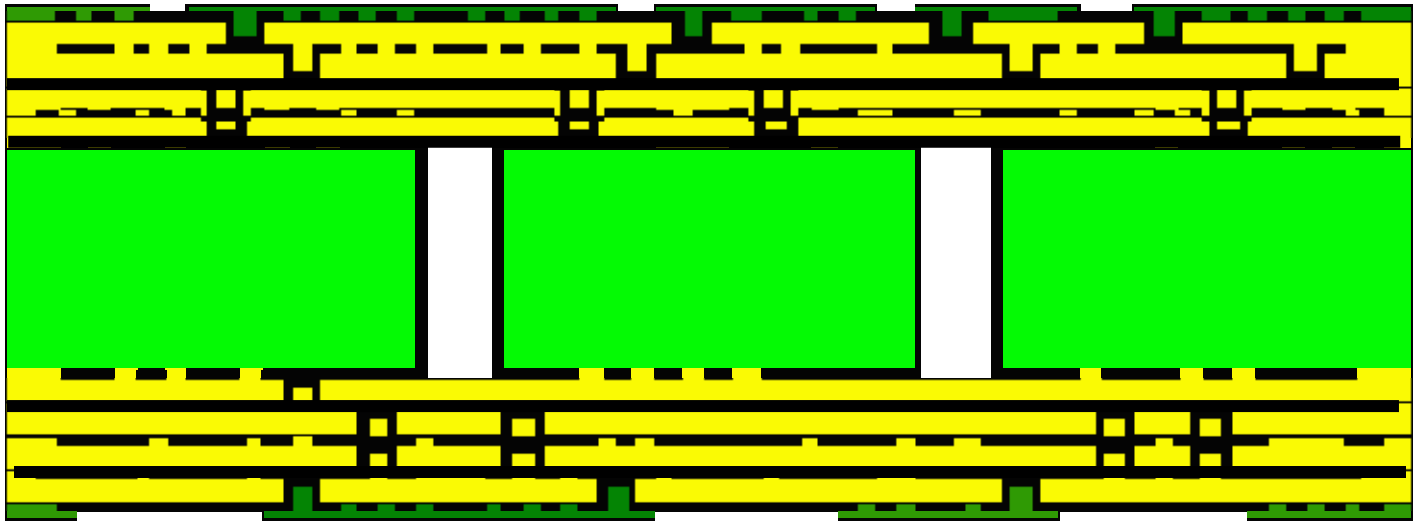


Virtex-4 FF1513 Pin-out

- New IO/Vcco/GND pattern
  - Better IO to GND/Vcco pair ratio
  - Every SelectIO adjacent to Vcco & GND

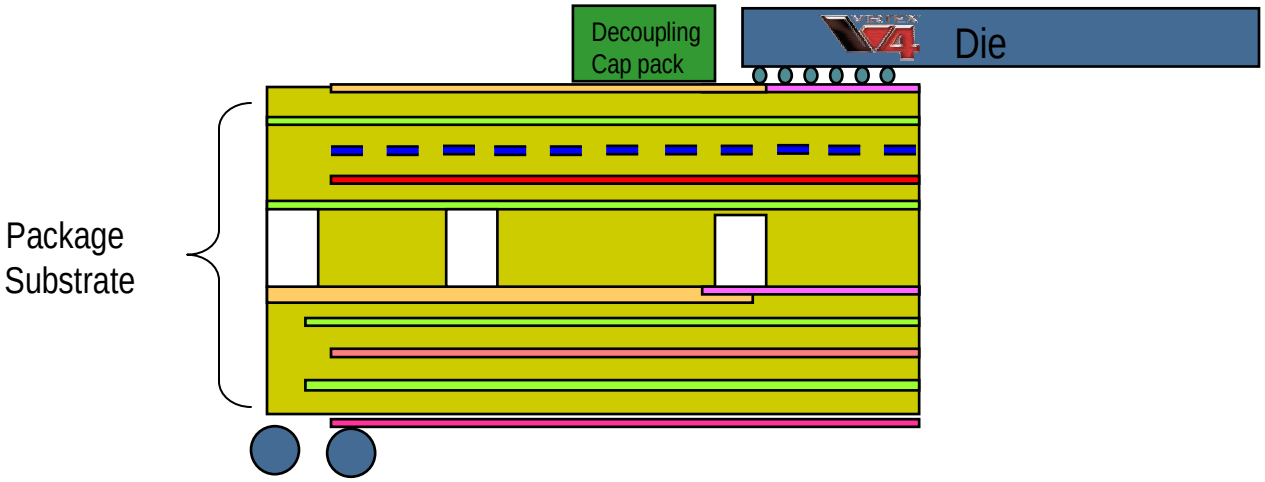
- Enhanced coupling of VCCint/GND pairs
- Checkerboard pin-out for minimum parasitic inductance

Virtex-4™ Package 10-Layer Stack-up



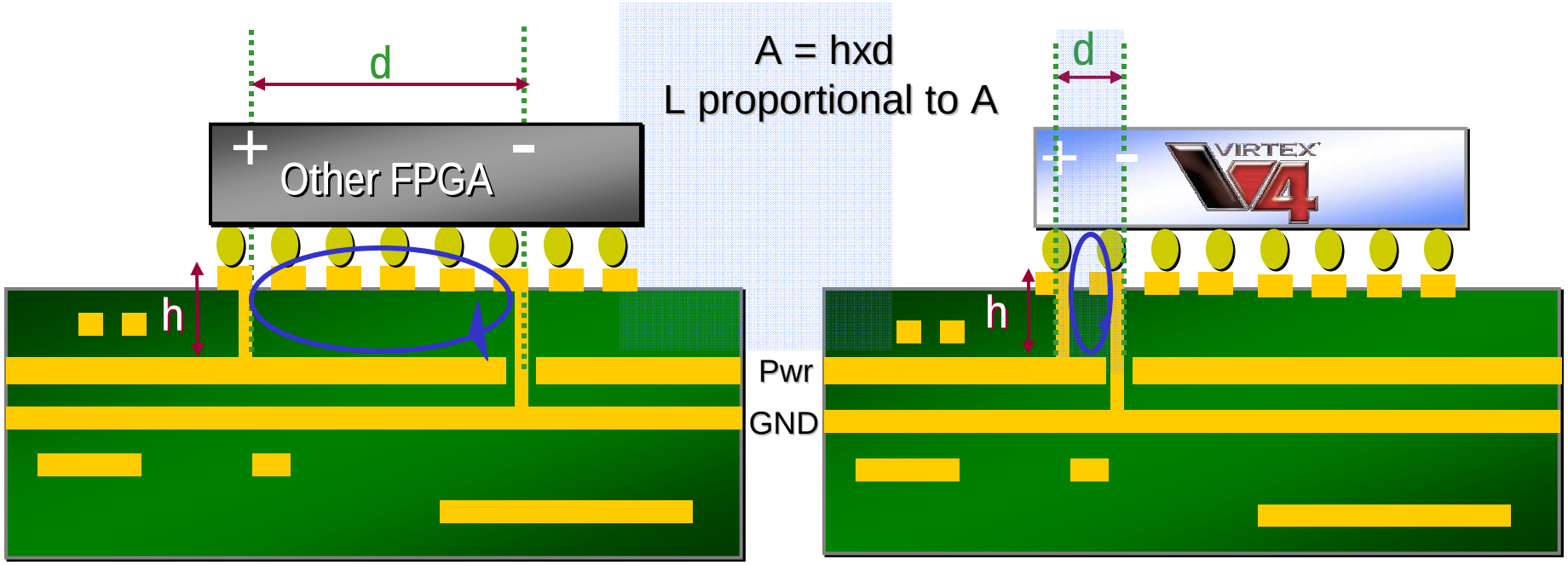
- Increase metal layer count from 6 to 10 and optimize stack-up
  - Allows for better plane continuity and better signal referencing
  - More liberal usage of power and ground vias to compliment signals during layer transitions within package

Power Distribution Improvements Planes and Decoupling



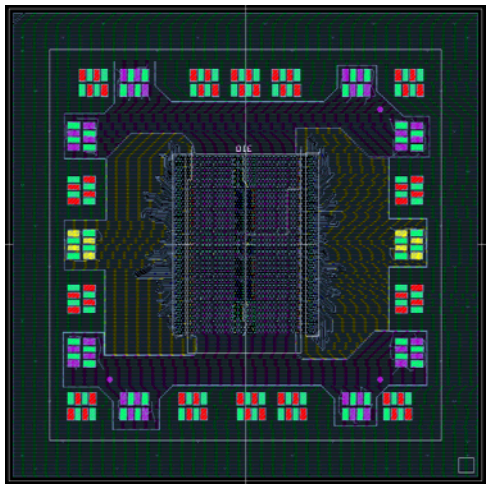
- New on-package low-intrinsic-inductance capacitors
  - Low inductance capacitor connections to package power planes
- Significantly improve high frequency response for package power system
  - Zo integrity – more robust controlled impedance transmission lines
  - Better reference plane continuity and lower effective plane inductance
  - Improved return path quality of these planes

Reduced Inductance Through Better GND & Power Coupling

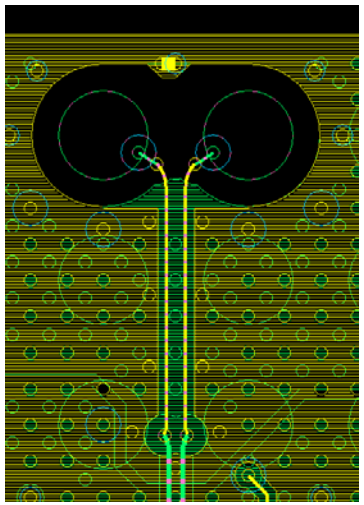


Smaller Current Loop Area Leads to reduced PCB Inductance (L)

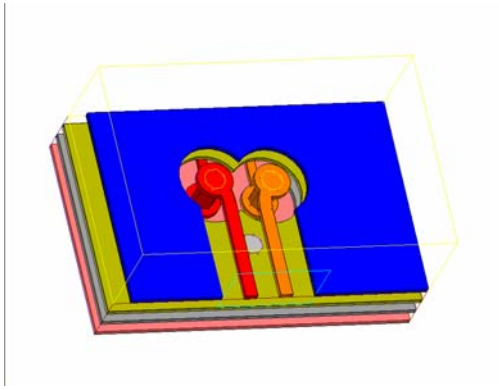
Extensive Package 3-D Modeling



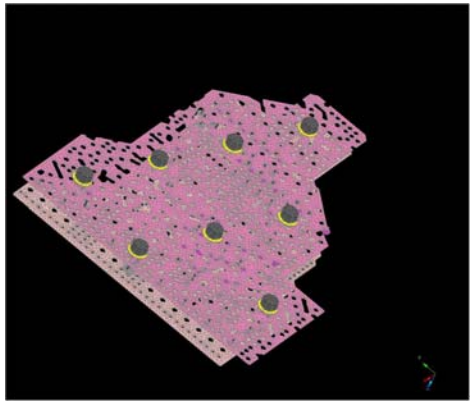
Allergro MCM file



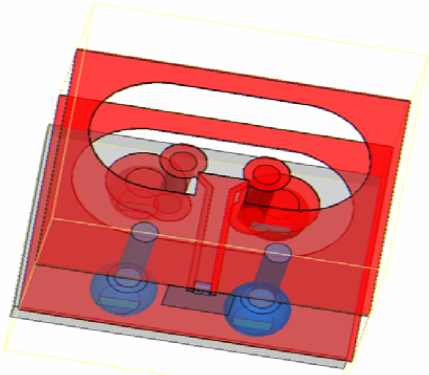
RocketIO routing at package edge



Package build-up layer vias for RocketIO signals



Virtex-4 Package Power and Ground Plane

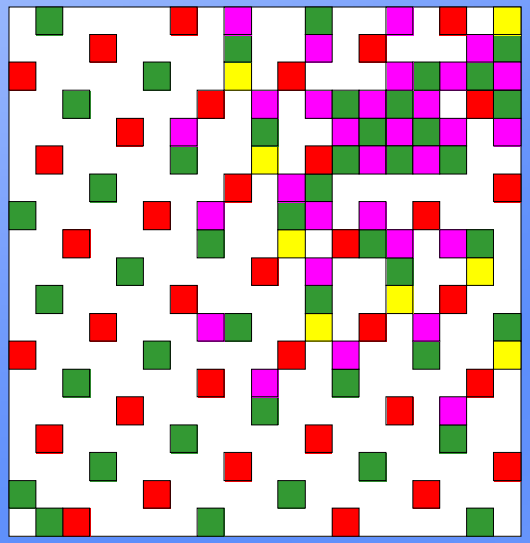


RocketIO - solder ball region

Better Ratio of I/O to Vcco/GND Pins

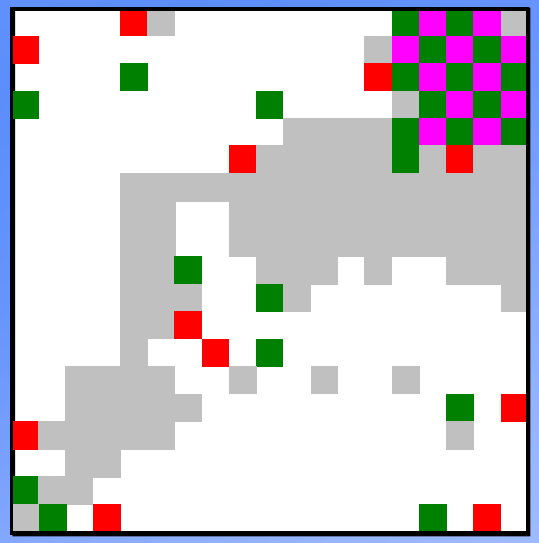
South-West Die Quadrant Comparison of Virtex-4 & Other FPGA

Virtex-4 FPGA



VCCo
GND
VCCint
VCCaux
I/O
Other

Other FPGA



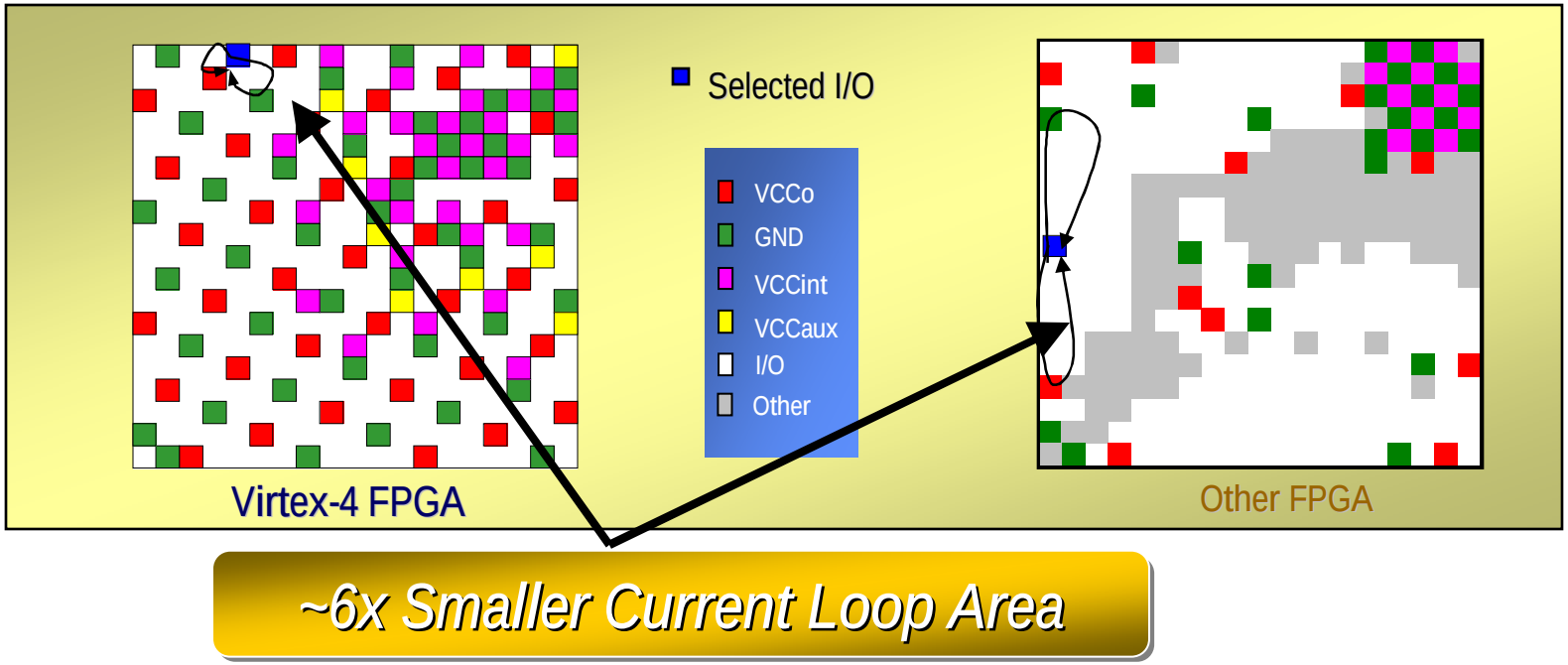
1 Vcco/GND pair per 9.4 I/Os

1 Vcco/GND pair per 20.45 I/Os

~2x better ratio of I/O to Vcco/GND pairs

Smaller Current Loop Area Leads to Better Power & Signal Integrity

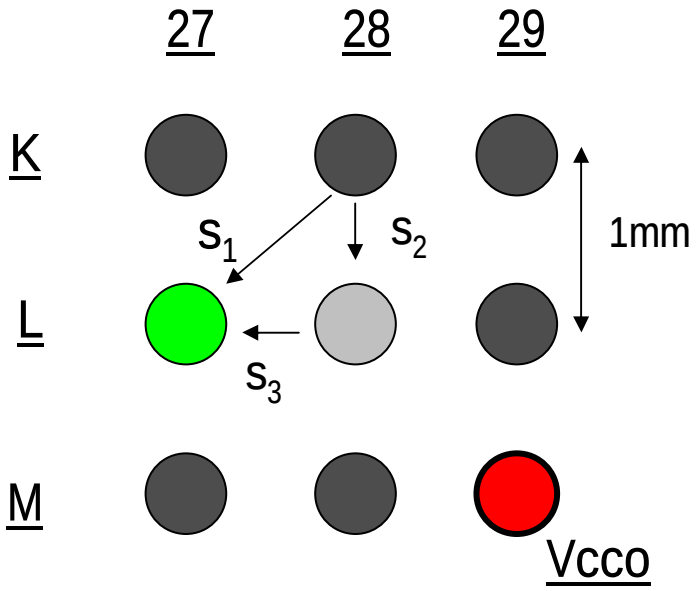
- Close coupling of I/O to GND/Vcco pair resulting in:
  - Smaller return current loop area
  - Reduced PCB and package inductance and reduced via crosstalk
  - Lower noise in the I/O power system and lower jitter & better signal integrity



Crosstalk Reduction through Improvement in I/O Signal Isolation

- Highest performance interface design reduces budgets for jitter and reference signal noise
  - Increased spacing of I/O signals, Voltage References (V_{REF}) and Clocks, resulting in lowest package coupling between signals
  - Increased package trace spacing up to 2x over the previous package design
- Greater than 2x I/O package coupling reduction

Xilinx SparseChevron™ Ball Pattern



Examine aggressor package ball at K28 coupling into the victim package ball at L28:

Here s_1 = 1.4 mm, s_2 = 1 mm,
s_3 = 1 mm, typical ball radius = .35 mm
Xilinx package balls 700 um diameter,
h = 700 um

$$L_m = h \times 200 \times \ln(s_1 s_3 / s_2 r)\ nH$$

$$L_m = 700\ um \times 200 \times \ln(1.4 \times 1.0 / 1.0 \times .35)\ nH$$
$$= .19\ nH$$

Similar calculations show other aggressors contribute as follows:
K27 = M27 = L_M of .1 nH
K29 = L_M of .21 nH
L29 = L_M of .24 nH
M28 = L_M of .19 nH

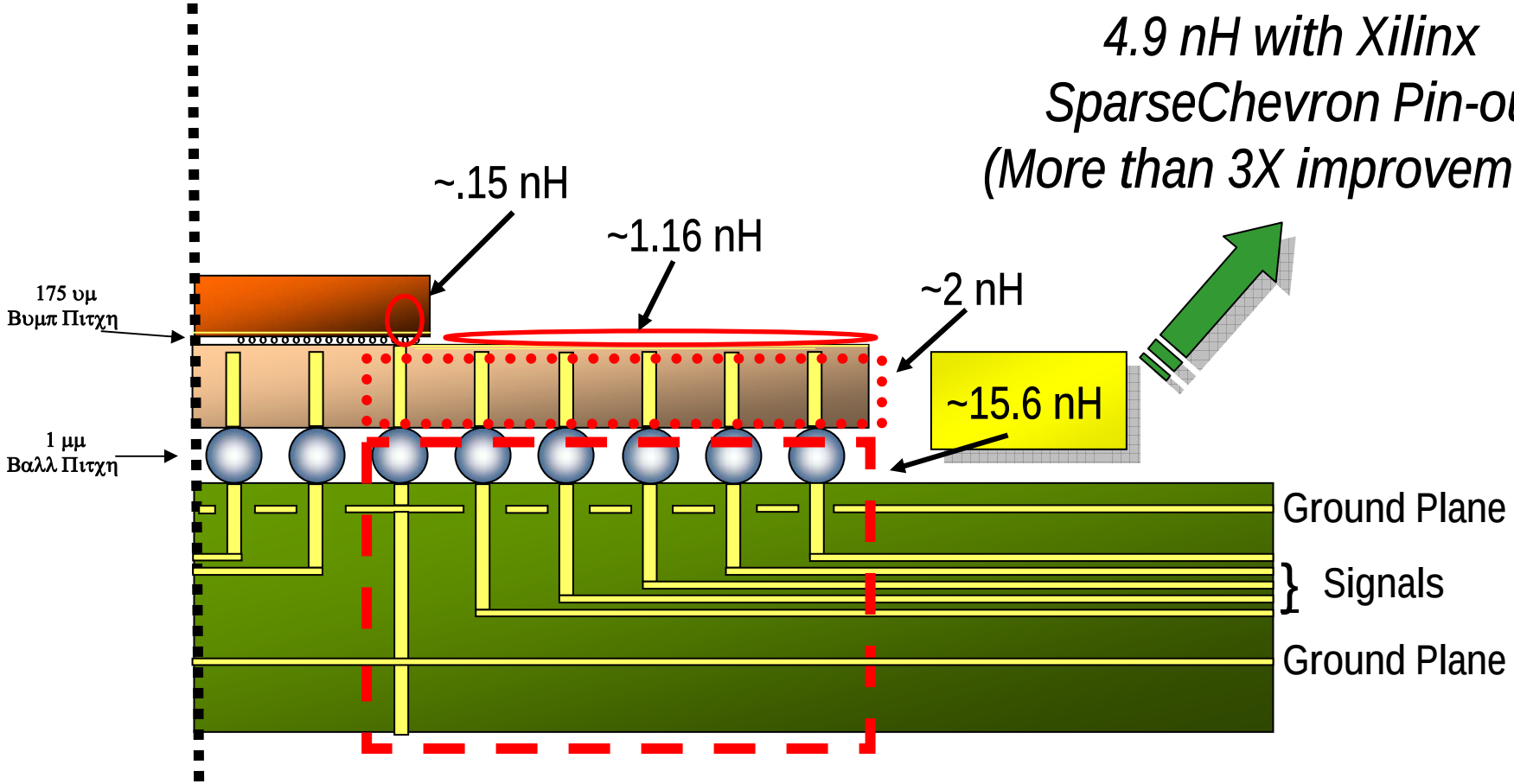
Top View of PCB Vias FF1148

- Victim Via
- Aggressor Via
- Shared Return (Ground) Via

Xilinx Advantages: Every IO near V_{CCO} & Ground; only 6 aggressors!

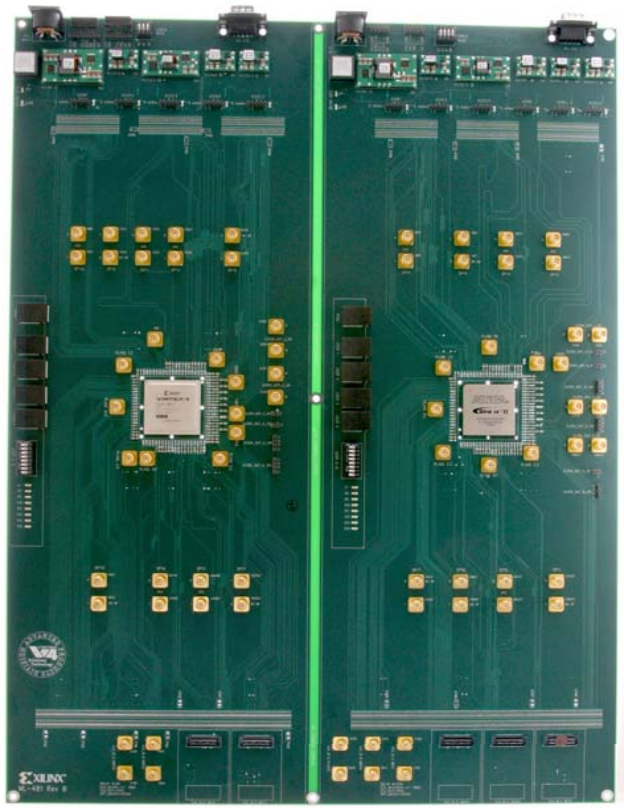
Breakout of Total Mutual Inductance

This number reduced to 4.9 nH with Xilinx SparseChevron Pin-out (More than 3X improvement!)



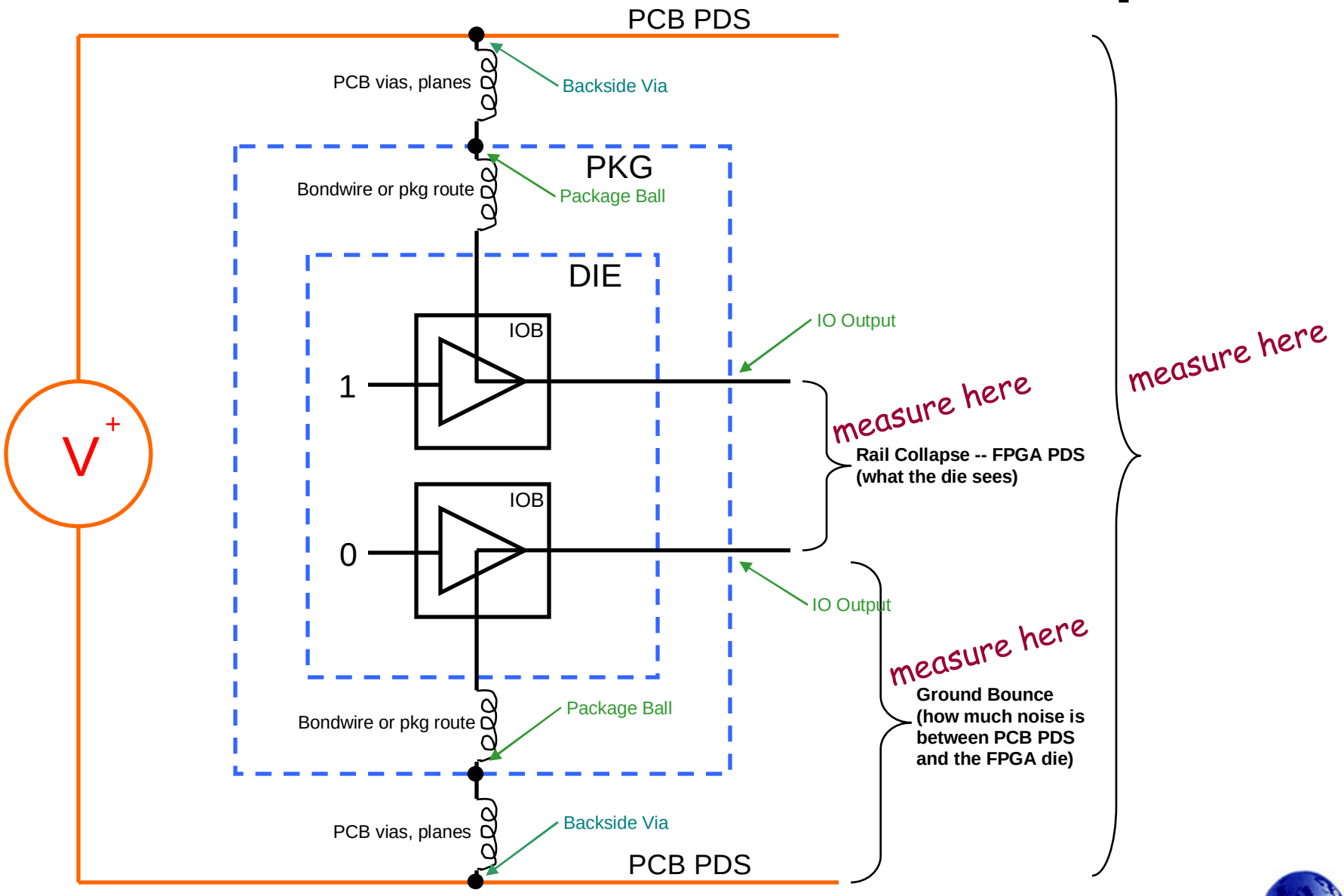
82% of Noise is determined by the Pinout and found in Package Balls and PCB vias

Hardware Measurements Confirm Packaging Benefits

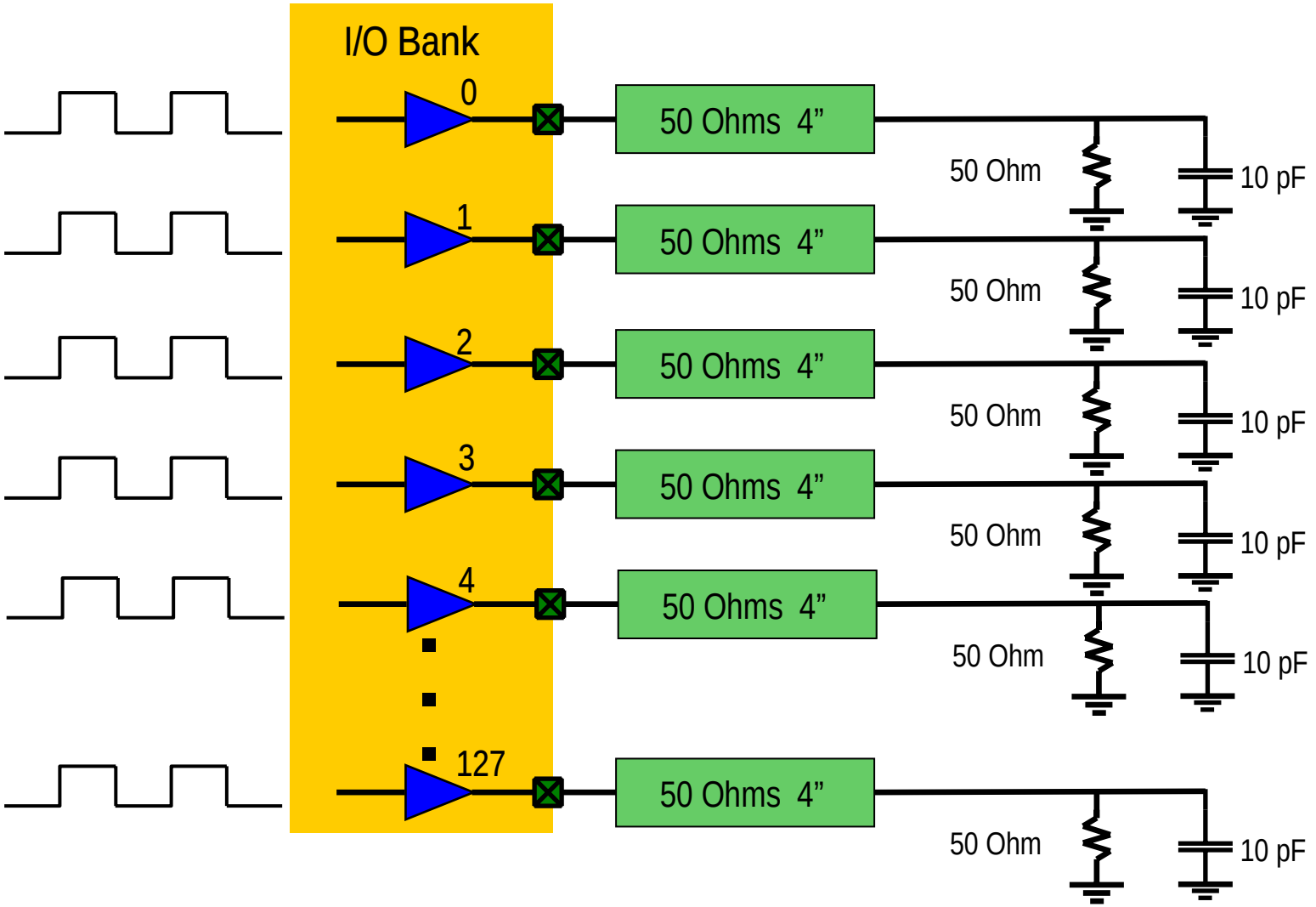


- ML481 Hardware Characterization Platform
  - 24-layer stack-up
  - 125-mil thick
  - 8 dedicated ground plane layers, 4 dedicated V_{CC} plane layers
  - Identical PDS decoupling networks, exceeding manufacturer's recommendations

ML481 Measurement Technique

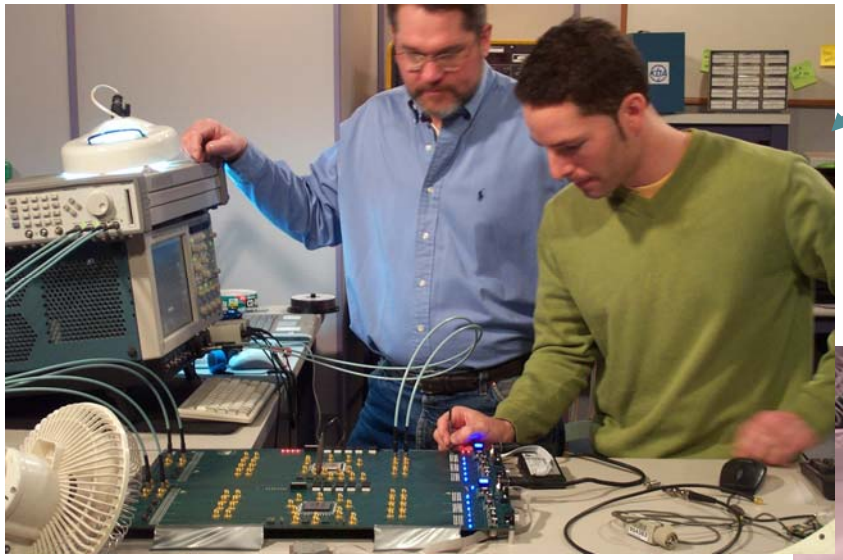


Test Pattern/Test Condition



Lab Setup

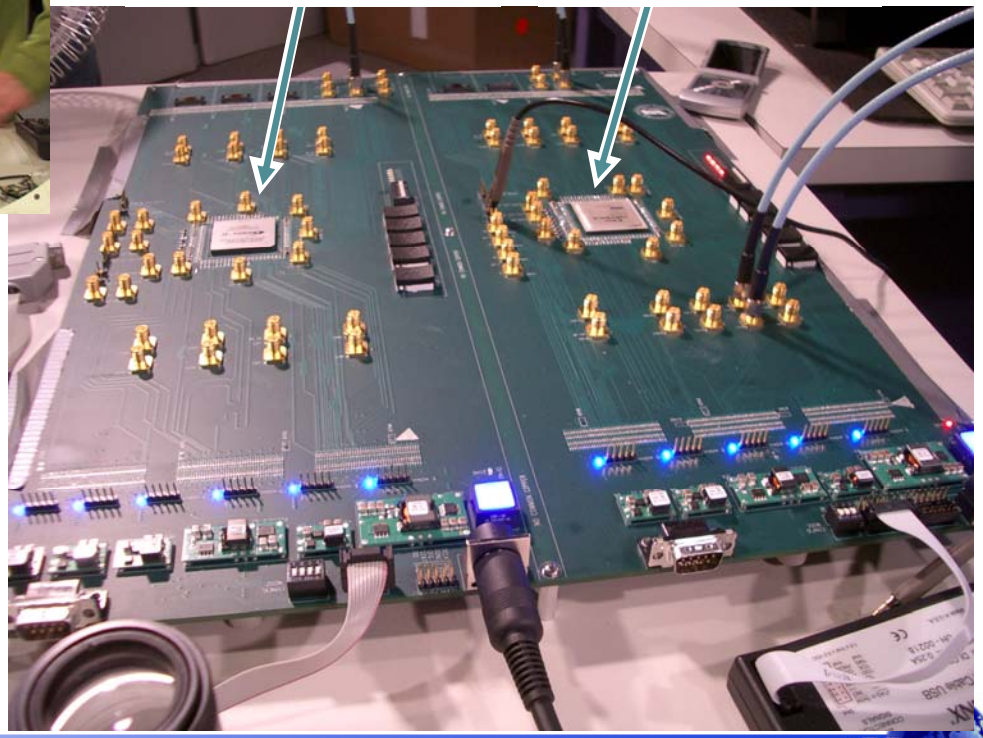
Dr. Howard Johnson



Mark Alexander (designed board)

Altera Stratix II
model 2S60
F1020 pkg.
32x32 BGA

Xilinx Virtex-4
model LX60
FF1148 pkg.
34x34 BGA



Isolated power for each side
(no common grounds)

- 24 layers
- 110 mil thick
- 3 I/O power regions
- 500 active I/O's

Source: Dr. Howard Johnson 3/1/05 TOL seminar

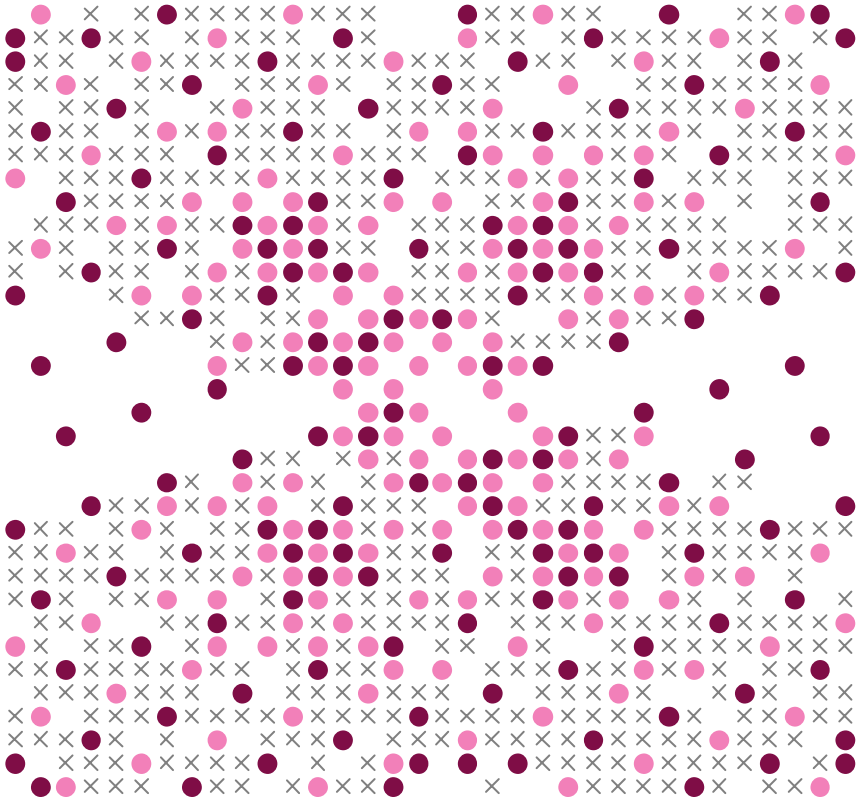
Three Measures of Crosstalk

- Spiral Test
  - 100 outputs, individual
- Accumulating Test
  - 100 outputs, accumulating
- Hammer Test
  - 500 outputs, all together at once

Source: Dr. Howard Johnson 3/1/05 TOL seminar

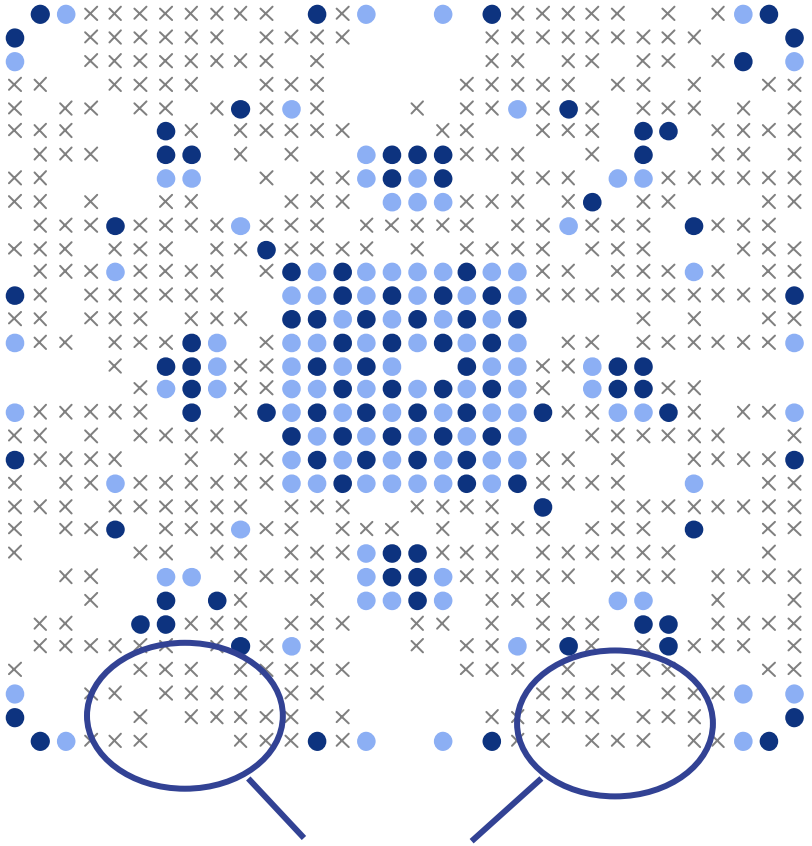
Package Comparison

Xilinx® Virtex™-4 FF1148



Returns spread evenly

Altera Stratix II F1020



Many regions devoid of returns

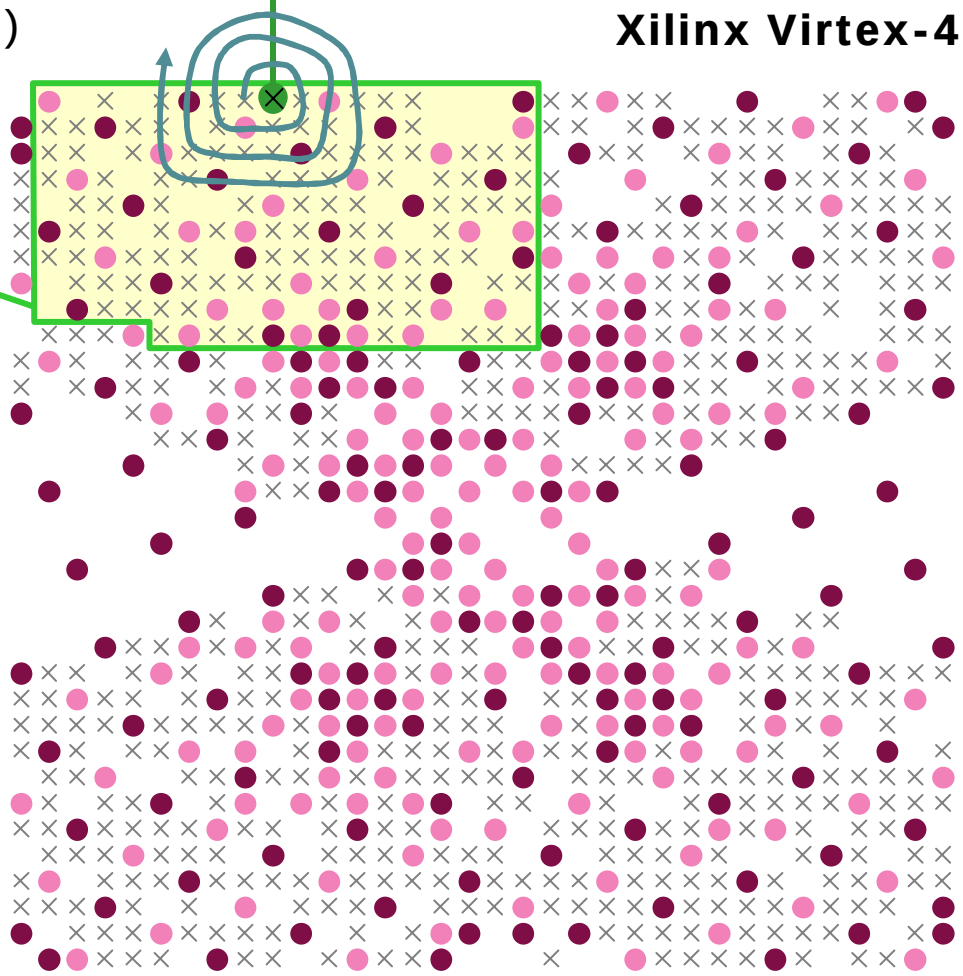
Source: Dr. Howard Johnson 3/1/05 TOL seminar

Spiral Test Pattern: Xilinx

Victim A10
(worst-case location)

Region exercised
by spiral test

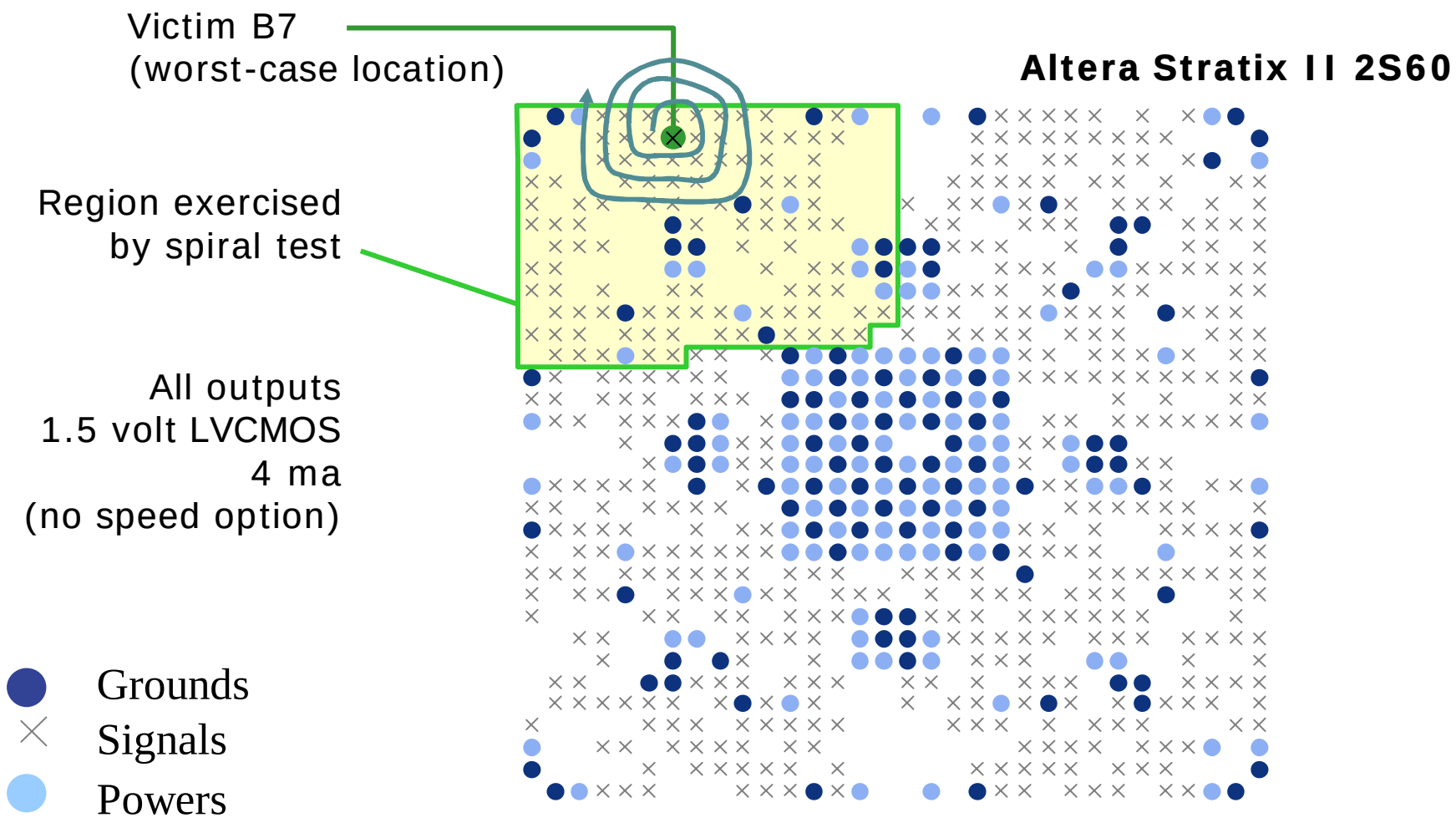
All outputs
1.5 volt LVCMOS
4 ma, *fast*



Grounds
Signals
Powers

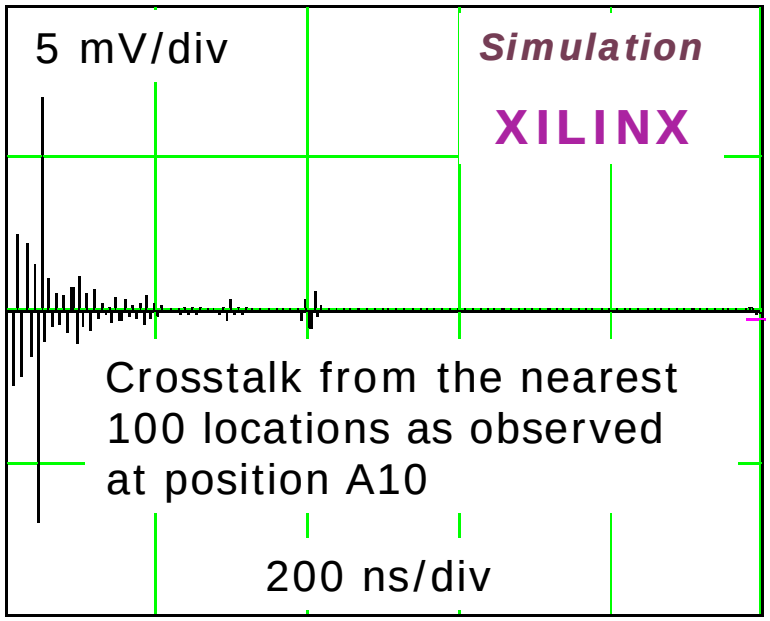
Source: Dr. Howard Johnson 3/1/05 TOL seminar

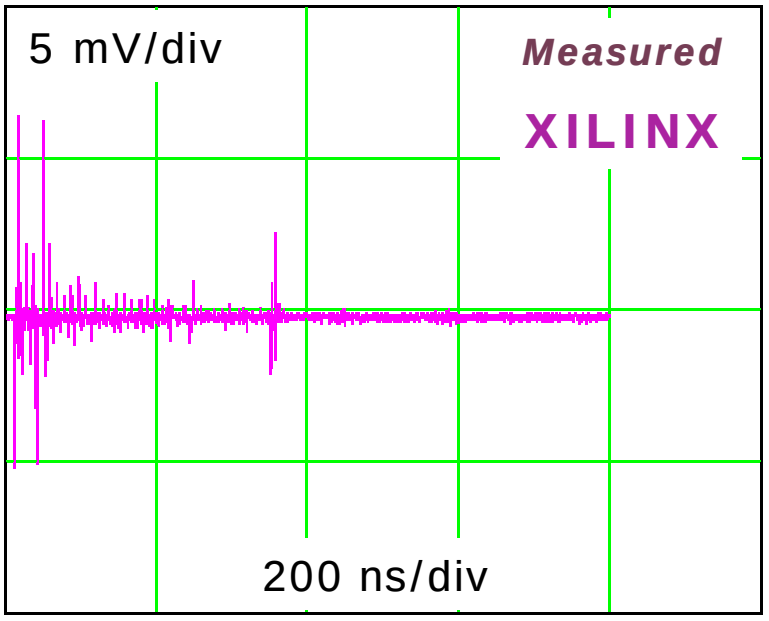
Spiral Test Pattern: Altera



Source: Dr. Howard Johnson 3/1/05 TOL seminar

Spiral Test Results: Simulation vs. Measurement





MathCad

- Signal positions
- Power/ground positions
- Signal amplitude and rise/fall time (di/dt)
- Trace depths

Tek TDS6804B Digital Storage Oscilloscope.
8 GHz bandwidth, 20 20Gbps Direct inputs with 40 inch semi hard-line SMA cables

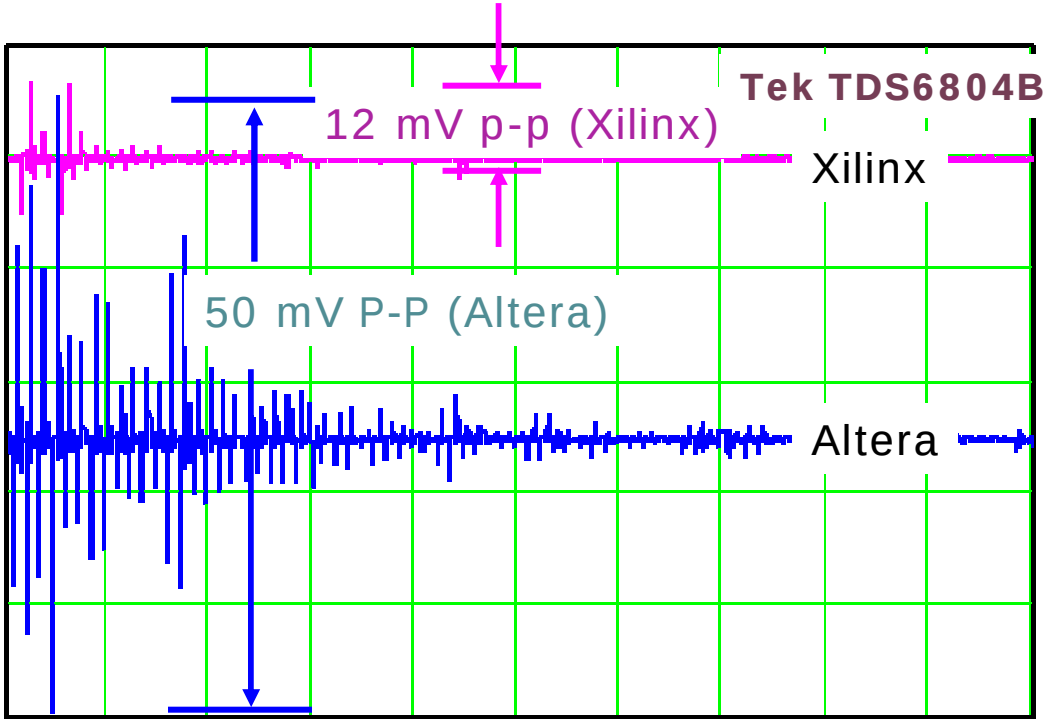
Source: Dr. Howard Johnson 3/1/05 TOL seminar

Spiral-Test Comparison

Xilinx: A10
1.5 volt LVCMOS
4 ma, *fast*

10 mV/div

Altera: B7
1.5 volt LVCMOS
4 ma
(no speed option)



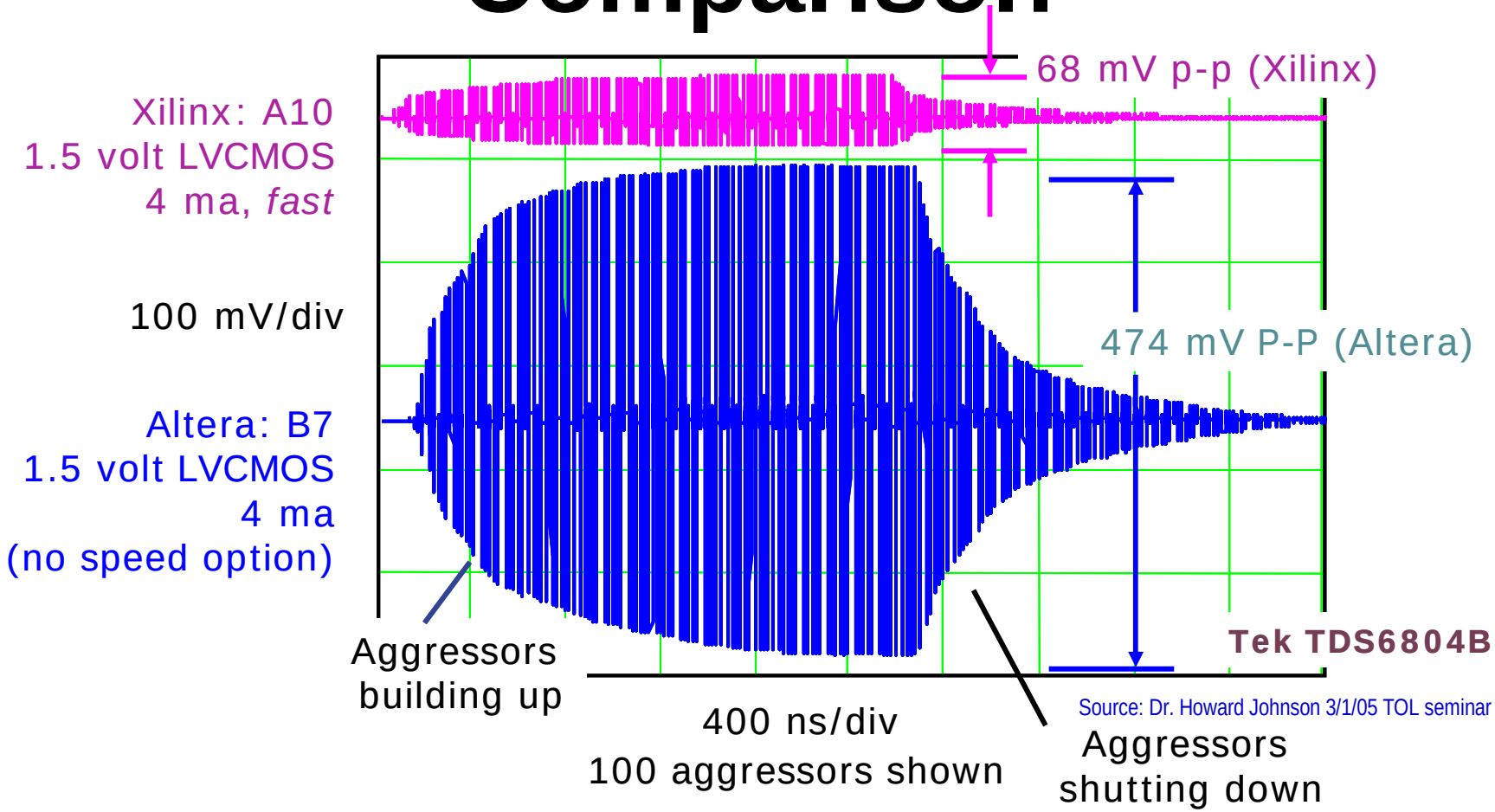
80 ns/div

100 aggressors shown

Source: Dr. Howard Johnson 3/1/05 TOL seminar

Up to 4X crosstalk reduction

Accumulating Test Comparison

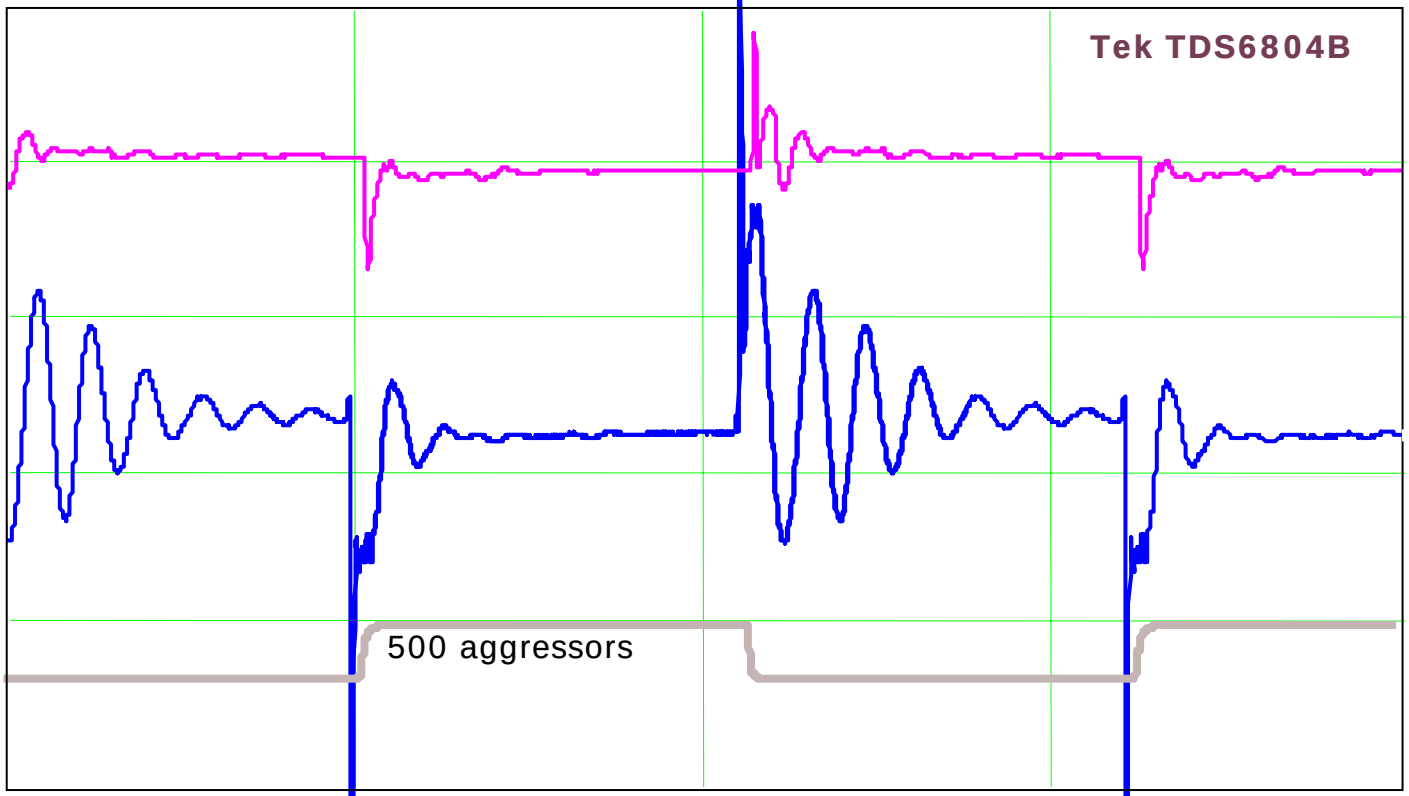


Source: Dr. Howard Johnson 3/1/05 TOL seminar

Up to 7X crosstalk reduction

Final Test: *The Hammer*

Up to 4.5 X crosstalk reduction

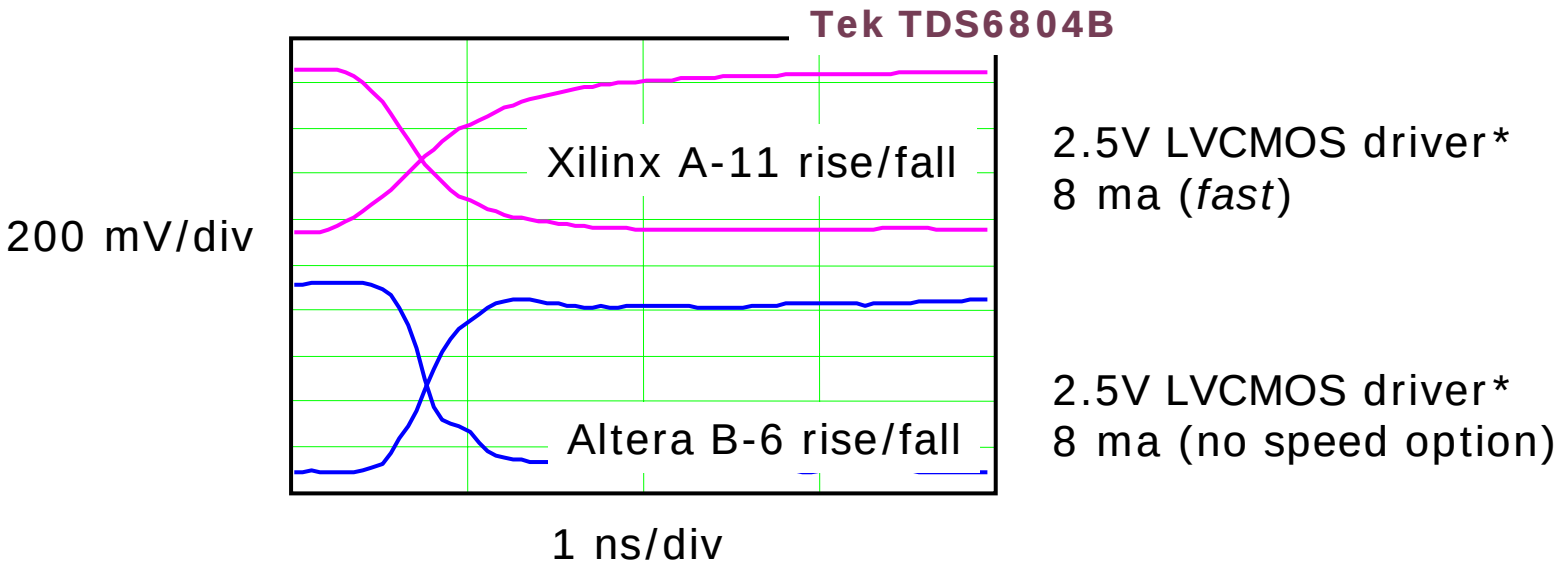


*powered by a range of voltages including 1.5-volt in the near field

Source: Dr. Howard Johnson 3/1/05 TOL seminar

(Waveforms time-shifted for visual clarity)

Rise/Fall Times



- The Altera component suffers from two artifacts:
  - Excessively fast rise/fall time
  - Over-concentration of power/ground balls in core region
- Together, these two effects combine to produce a 4.5:1 ratio of observed crosstalk in the hammer test.

Source: Dr. Howard Johnson 3/1/05 TOL seminar

*powered by 1.5V

Industry Expert Validates Virtex™-4 Signal Integrity Advantage

BGA Crosstalk

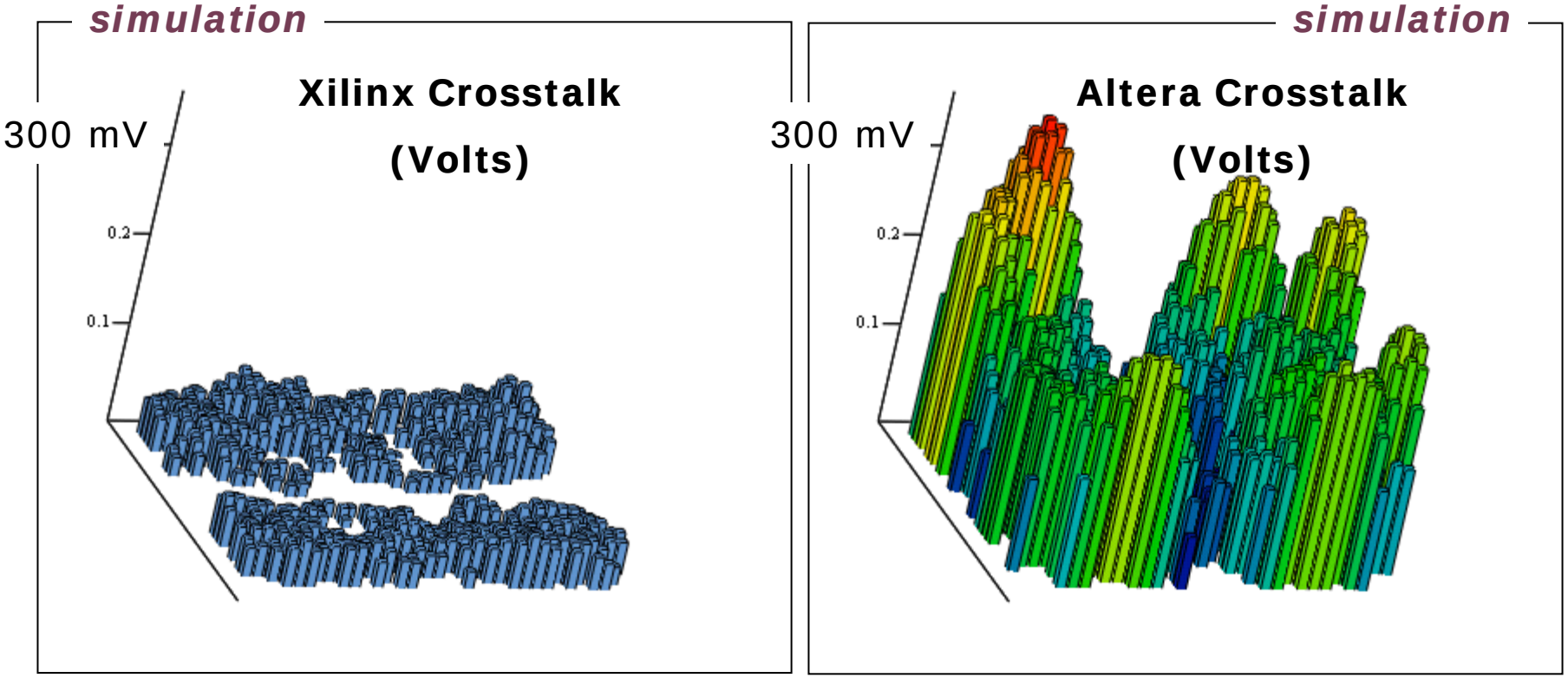
Xilinx Virtex-4 and Altera Stratix II Comparison
Prepared for Xilinx
Tech On-Line
March 1, 2005
By
Dr. Howard Johnson

slide 3.1

Crosstalk Measurement	Test detail	Stratix II Result	Virtex-4 Result	Virtex-4 SI Advantage
Spiral Test	100 outputs, individual	50 mV	12mV	over 4x crosstalk reduction
Accumulating Test	100 outputs switching, accumulating	474 mV	68 mV	7x crosstalk reduction
Hammer Test	500 outputs, all switching simultaneously	572 mV	123 mV	over 4.5x crosstalk reduction

Achieved Technical Seminar available at http://www.xilinx.com/events/webcasts/tol/01feb05.htm#3

Simulated Package Performance

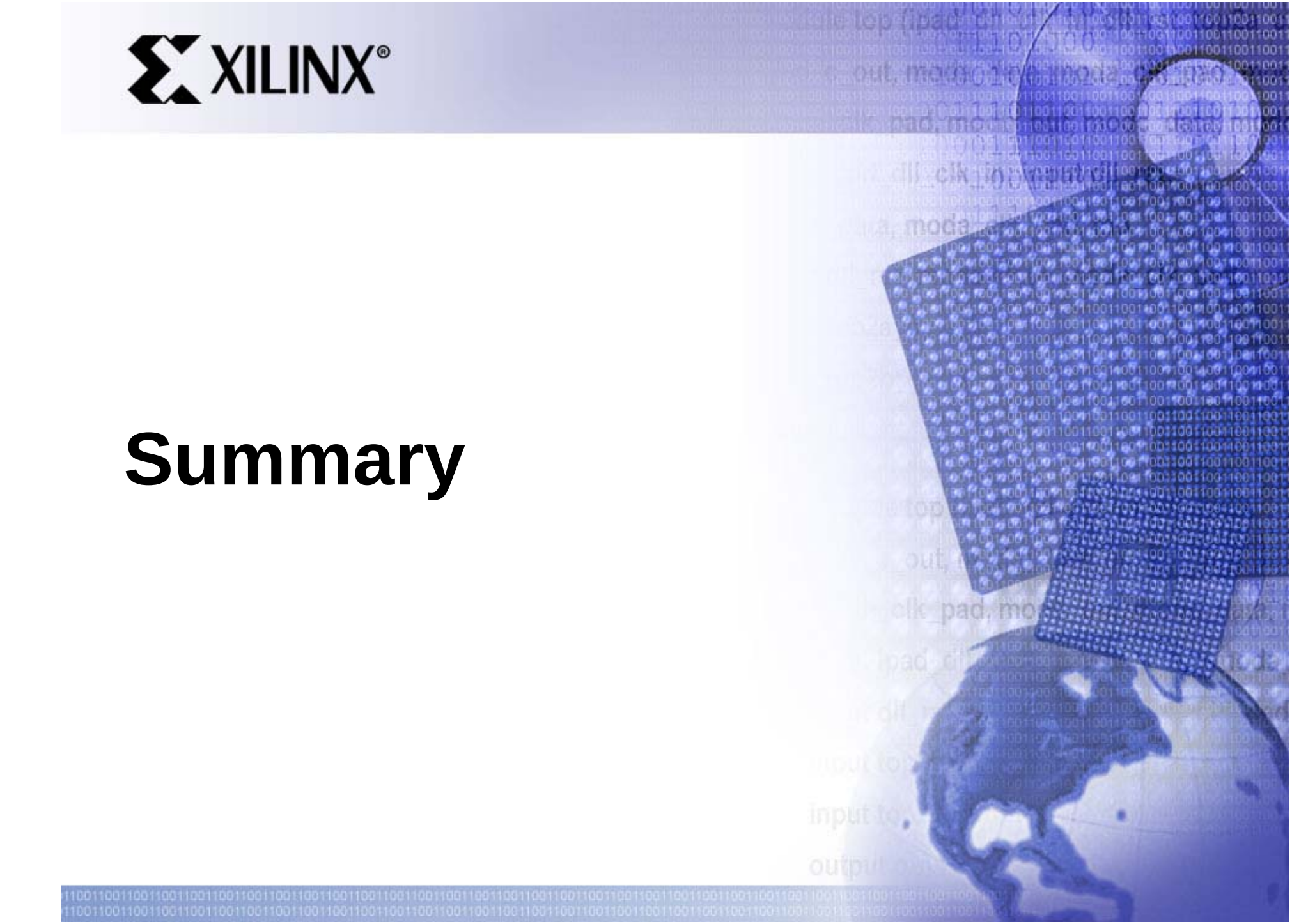


•Simulation assumes all outputs generate di/dt=2E+07 A/s; Consistent via depth of 0.035 in.; Via-in-pad

Source: Dr. Howard Johnson 3/1/05 TOL seminar

Delivers significant crosstalk reduction across the package with the same edge rate comparison

Summary



Virtex-4 Advanced Packaging Summary

- Noise is a big issue in high speed wide single-end interfaces (e.g. DDR2, QDR Memory Interfaces)
- Good package design is critical to solve the SI challenge (e.g. SparseChevron™ package)
  - Optimized distribution of V_{CC} and GND pins for low inductance
  - Better substrate, bypassing, and signal trace isolation
- Designed & verified with extensive simulation & characterization
- Xilinx worked with industry renowned SI expert Dr. Howard Johnson to validate design
- Virtex-4 with SparseChevron package exhibits 4X-7X lower SSO noise than Competition

The Best Packaging Design for High Pin-Count 90nm FPGAs